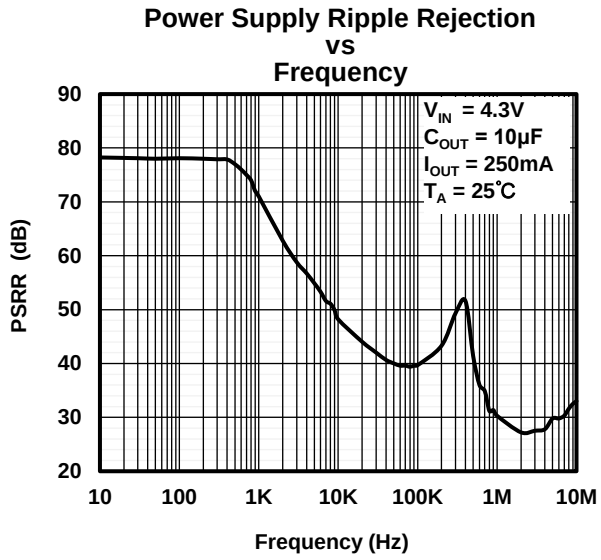
ULTRA LOW QUIESCENT CURRENT 250mA LOW-DROPOUT VOLTAGE REGULATORS

FEATURES

- **250mA Low-Dropout Voltage Regulator**
- **Dropout Voltage of 230mV (TYP) at 250mA**
- **Ultra-Low 36μA Typical Quiescent Current**
- **3% Tolerance over Specified Conditions**
- **Open Drain Power Good Output**
- **Compatible with Low ESR Capacitor**
- **Thermal Shutdown Protection**
- **8 Pin SOP Package**

APPLICATIONS

- **Battery-Powered Applications**
- **Power Converter/Inverter**
- **Portable Devices**



PRODUCT DESCRIPTION

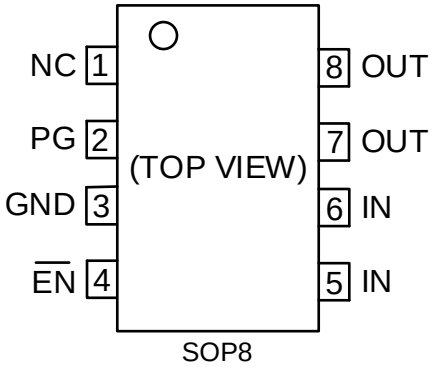
The TS6112-33 is designed to have ultra-low quiescent currents and be stable with very low ESR output capacitors with a wide range of capacitance (0.47μF or greater). The combination of the above characteristics allows for a small ceramic capacitor to be used at the output with high dynamic performance at low cost.

The TS6112-33 is designed with very low dropout voltages. The quiescent current is very low at light load (typically 36μA at 10uA load), however, it is designed to be dependent of output loading (approximately 1/250 of the output current at heavy load), in order to provide much improved transient response over competitions. The low quiescent feature yields a significant improvement in operating life for battery-powered systems. This LDO also features a sleep mode; applying a TTL high signal to $\overline{EN}$ (enable) shuts down the regulator, reducing the quiescent current to less than 1μA (typ).

Power good (PG) is an active high output, which can be used to implement a power-on reset or a low-battery Indicator.

Output voltage tolerance is specified as a maximum of 3% over line, load, and temperature ranges. The TS6112-33 is available in 8 pin SOP package.

PIN CONFIGURATION AND FUNCTIONS



TERMINAL		I/O	DESCROPTION
NAME	NO		
$\overline{EN}$	4	I	Enable Input
NC	1	I	No Connect for Fixed Option
GND	3		Regulator Ground
IN	5	I	Input Voltage
IN	6	I	Input Voltage
OUT	7	O	Regulated Output Voltage
OUT	8	O	Regulated Output Voltage
PG	2	O	PG Output

TYPICAL APPLICATION

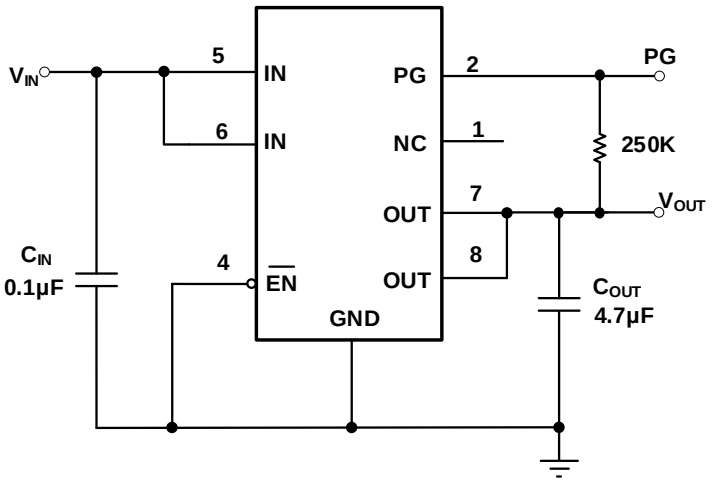


Figure 1. Typical Application Configuration for Fixed Output Options

RECOMMENDED OPERATING CONDITIONS

Parameter		MIN	MAX	UNIT
V_{IN} [1]	Input Voltage	2.7	12	V
V_{OUT}	Output Voltage Range	1.2	5	V
I_{OUT} [2]	Output Current	0	250	mA
T_J [2]	Operating Virtual Junction Temperature	-40	125	°C

[1] To calculate the minimum input voltage for your maximum output current, use the following equation: $V_{IN\_min} = V_{OUT\_max} + V_{DO\_max\ load}$, where V_{DO} is the dropout voltage.
[2] Continuous current and operating junction temperature are limited by internal protection circuitry, but it is not recommended that the device operate under conditions beyond those specified in this table for extended periods of time.

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted) [3]

Parameter	Min	Max	Unit
Input Voltage Range	-0.3	14	V
Voltage Range at $\overline{EN}$	-0.3	16.5	V
PG Voltage		16.5	V
Peak Output Current	Internally Limited		
Output Voltage, V_{OUT}		7	V
Junction Temperature	-40	125	°C
Storage Temperature Range	-65	150	°C
ESD HBM		±4000	V
ESD MM		±200	V
ESD CDM		±1000	V

[3] Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING INFORMATION

Model	Part Number	Eco Plan	Package	Output Voltage (V)	Container, Pack Qty
TS6112-33	TS611233SOP8R	RoHS	SOP8	3.3	Reel, 2500

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjects to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

ELECTRICAL CHARACTERISTICS

At T_J = +25˚C, V_{IN} = V_{OUT} (typ.) + 1 V, I_{OUT} = 10μA, $\overline{EN}$ = 0V, C_{OUT} = 4.7μF (unless otherwise noted)
Boldface limits apply over the specified Junction temperature range, **T_J = −40˚C to +125˚C.**

Parameter		Operating Conditions	Min	Typ	Max	Unit
V_{OUT}	Output Voltage [4] (10μA to 250mA Load)	4.3 ≤ V_{IN} ≤ 12V		3.3		
		T_J = −40˚C to +125˚C	**3.2**		**3.4**	
I_{GND}	Quiescent Current [4] (GND Current)	$\overline{EN}$ = 0V		36		μA
		T_J = −40˚C to +125˚C			**60**	
Output Voltage Line Regulation [4][5] ($\Delta V_O/V_O$)		V_{OUT} + 1V ≤ V_{IN} ≤ 12V,		0.005		%/V
Load Regulation		**I_{OUT} = 10μA to 250mA** **T_J = −40˚C to +125˚C**		**0.5%**		
Output Noise Voltage		BW = 300Hz to 50kHZ, C_{OUT} = 4.7μF		150		μVrms
Output Current Limit		V_{OUT} = 0V		0.78		A
Thermal Shutdown Junction Temperature				150		˚C
Thermal Shutdown Hysteresis Temperature				20		˚C
I_{STB}	Standby Current	$\overline{EN}$ = V_{IN} , 2.7V ≤ V_{IN} ≤ 12V		1		μA
		T_J = −40˚C to +125˚C			**10**	
V_{IH_EN}	High Level Enable Input Voltage	**T_J = −40˚C to +125˚C**	**2**			V
V_{IL_EN}	Low Level Enable Input Voltage	**T_J = −40˚C to +125˚C**			**0.8**	V
PSRR	Power Supply Ripple Rejection [3]	f = 1kHz, I_{OUT} = 10μA, C_{OUT} = 4.7μF		67		dB
PG	Minimum Input Voltage for Valid PG	$I_{OUT\ (PG)}$ = 300μA		1.25		V
	Trip Threshold Voltage	**V_{OUT} Decreasing** **T_J = −40˚C to +125˚C**	**92**		**98**	%/V_{OUT}
	Hysteresis Voltage	Measured at V_{OUT}		0.5		%/V_{OUT}
	Output Low Voltage	V_{IN} = 2.7V, I_{OUT}(PG) = 1mA		0.16		V
	Leakage Current	**$V_{(PG)}$ = 5 V** **T_J = −40˚C to +125˚C**			**1**	μA
I_{EN}	Input Current ($\overline{EN}$)	$\overline{EN}$ = 0V	-1		1	μA
		$\overline{EN}$ = V_{IN}	-1		1	μA
V_{DO}	Dropout Voltage [6]	I_{OUT} = 250mA		230		
		T_J = −40˚C to +125˚C			**400**	

[4] Minimum IN operating voltage is 2.7V or V_{OUT} (typ.) + 1V, whichever is greater. Maximum IN voltage is 12V.
[5] If V_{OUT} < 1.7V then V_{IN_min} = 2.7V, V_{IN_max} = 12V：

$$\Delta V_{OUT}\ (mV) = \text{Line Reg. } (\%/V) \times \frac{V_{OUT} \times (V_{IN\_max} - 2.7V)}{100} \times 1000$$

If V_{OUT} ≥ 1.7V then V_{IN_min} = V_{OUT} + 1V, V_{IN_max} = 12V：

$$\Delta V_{OUT}\ (mV) = \text{Line Reg. } (\%/V) \times \frac{V_{OUT} \times (V_{IN\_max} - (V_{OUT} + 1V))}{100} \times 1000$$

[6] IN voltage equals V_{OUT} (typ.) – 100mV, TS6112-33 input voltage needs to drop to 3.2V for purpose of this test.

TABLE OF GRAPHS

Parameter		FIGURE
Output Voltage	vs Load Current	2
	vs Free-Air Temperature	3
Ground Current	vs Load Current	4
	vs Free-Air Temperature	7
Dropout Voltage	vs Free-Air Temperature	5
Power Supply Ripple Rejection	vs Frequency	6
Line Transient Response		8
Load Transient Response		9
Output Voltage	vs Time	10
Output Spectral Noise Density	vs Frequency	11

TYPICAL CHARACTERISTICS

At T_A = +25˚C, V_S = 5V, R_L = 10kΩ connected to V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

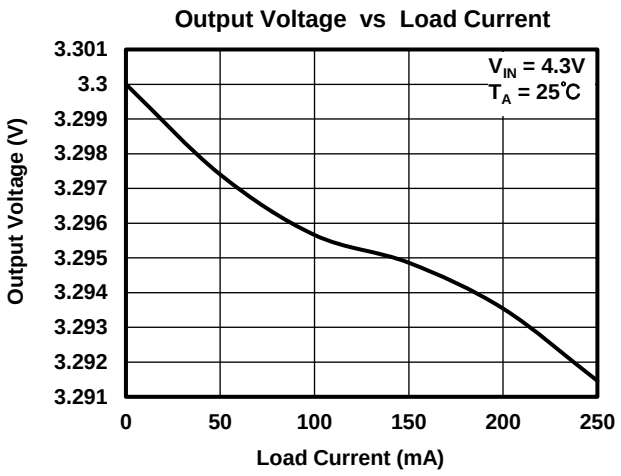


Figure 2.

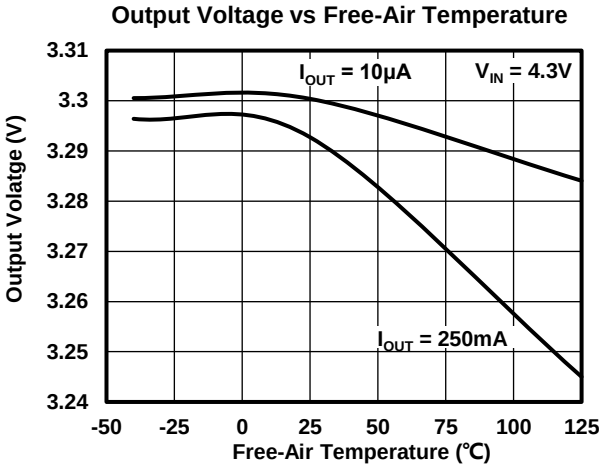


Figure 3.

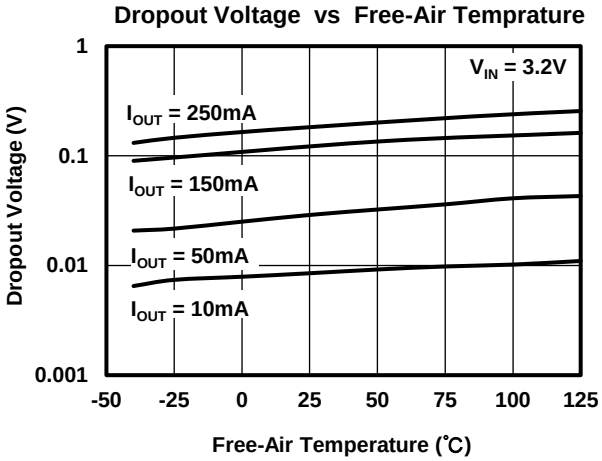


Figure 4.

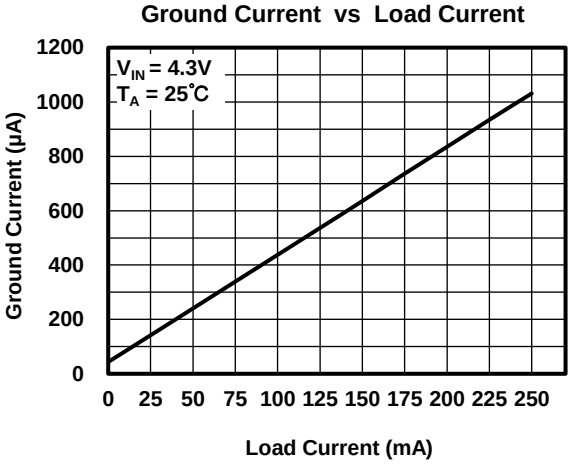


Figure 5.

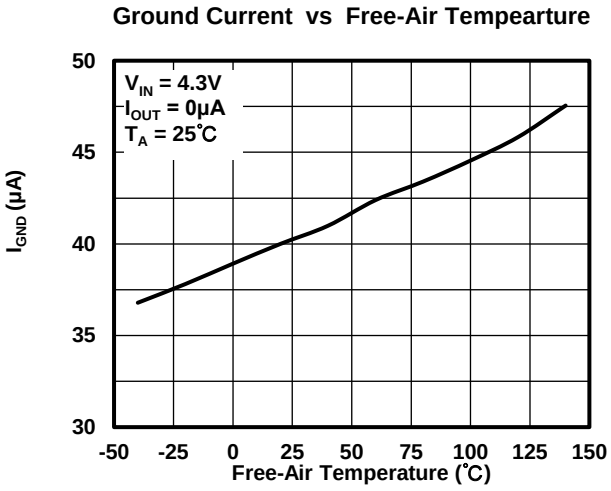


Figure 6.

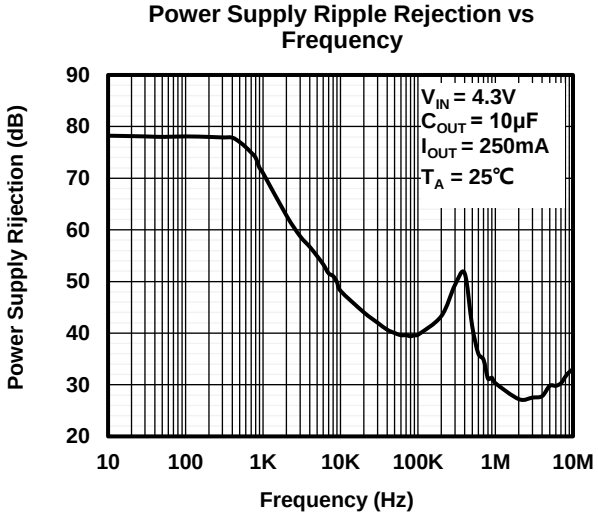


Figure 7.

TYPICAL CHARACTERISTICS (CONTINUE)

At T_A = +25°C, V_S = 5V, R_L = 10kΩ connected to V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

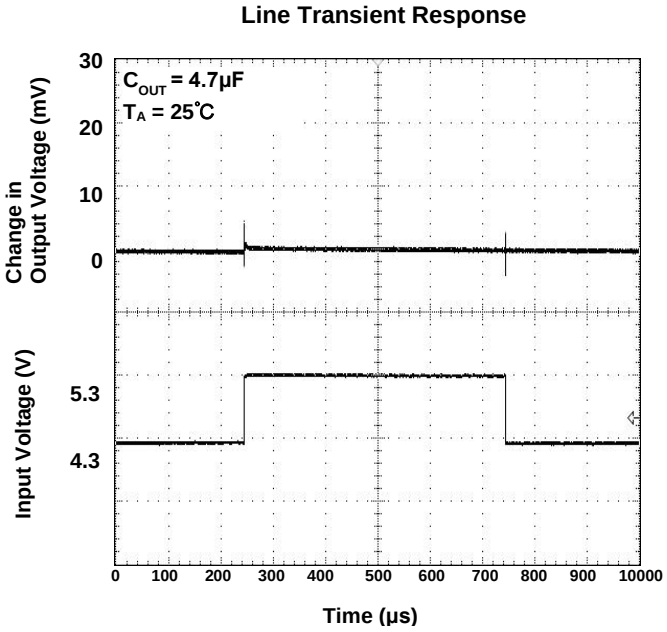


Figure 8.

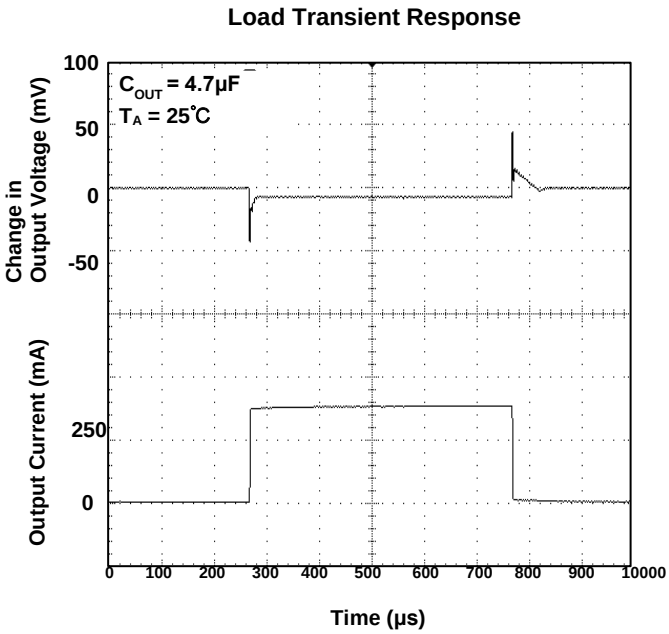


Figure 9.

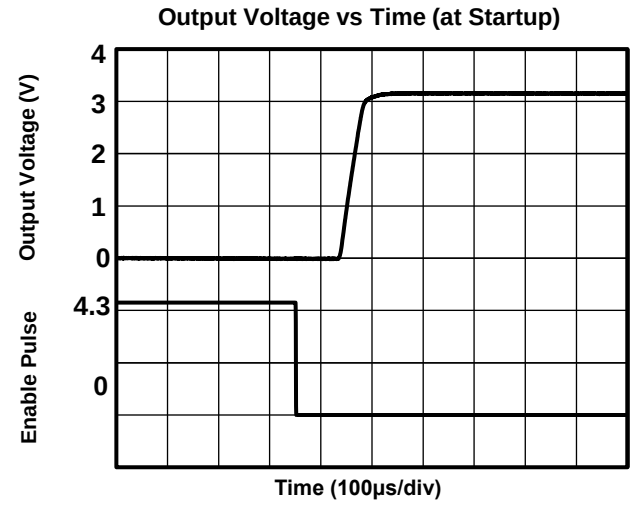


Figure 10.

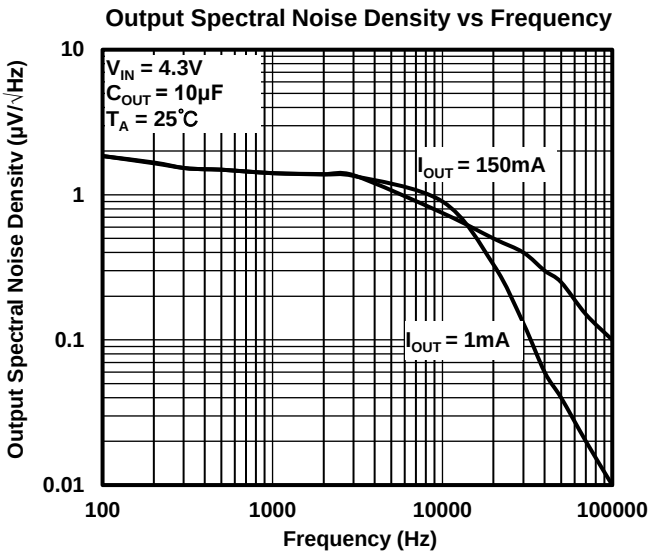


Figure 11.

APPLICATION INFORMATION

A typical application circuit is shown in Figure 12.

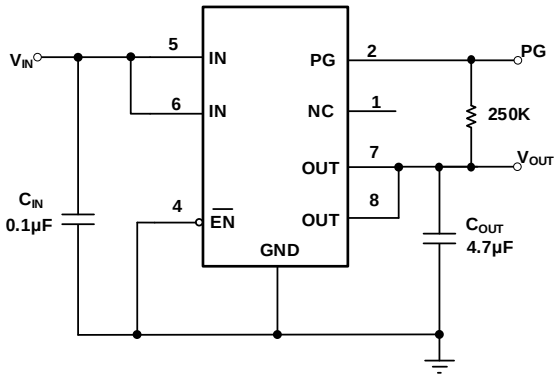


Figure12. Typical Application Circuit (Fixed Version)

Device Operation

The TS6112-33 features very low quiescent current at light load (typically 36µA at 10µA load), however, it is designed to be dependent of output loading (approximately 1/250 of the output current at heavy load), in order to provide much improved transient response over competitions. This dependency hardly has any effect on the operation efficiency at light or heavy load. When load current approaches the maximum output current (250mA), the ground pin current will only be approximately 1mA, which is independent of the supply voltage.

Unlike a linear regulator with a PNP-pass device, which tends to saturate when the **regulator** goes into dropout resulting in an increase in quiescent current even at light load or no load, TS6112-33 uses PMOS transistor as the pass device and a proprietary circuit technique to prevent quiescent current from going up when regulator is in dropout condition. In battery-powered systems, it means longer lasting battery even when the voltage decays below the minimum required for regulation.

The TS6112-33 family also features a shutdown mode that places the output in the high-impedance state (essentially equal to the feedback-divider resistance) and reduces quiescent current to 1µA (typ). If the shutdown feature is not used, $\overline{EN}$ should be tied to ground. Response to an enable transition is quick; regulated output voltage is reestablished in typically 160µs.

Minimum Load Requirements

The TS6112-33 is stable even at zero load; no minimum load is required for operation.

External Capacitor Requirements

The input capacitor is not required usually, however, a ceramic bypass capacitor (0.047µF or greater) improves load transient performance and overall loop stability. A higher capacitance capacitor may be necessary if large load transients with fast rise times are anticipated.

The TS6112-33 requires an output capacitor to stabilize the feedback loop, however, the often seen minimum ESR (the equivalent series resistance) requirement for the output capacitor is not applicable. Instead, the ESR should be limited to under 1Ω for the benefit of stability under large load current. The capacitance of the output capacitor should be greater than 0.47µF, though the recommended capacitance for this capacitor is 4.7µF or larger. Due to the characteristics of low ESR even at low temperatures, ceramic, solid tantalum and solid aluminum electrolytic capacitors are all suitable for TS6112-33. When non-solid electrolytic capacitors are used, especially for low temperature applications, it is strongly recommended that a ceramic capacitor with values greater than 0.47µF be connected in parallel.

APPLICATION INFORMATION

Power-Good Indicator

The TS6112-33 features a power-good (PG) output that can be used to monitor the status of the regulator. Internal comparator monitors the output voltage: when the output drops to between 92% and 98% of its nominal regulated value, the PG output transistor turns on, taking the signal low. The open-drain output requires a pullup resistor, it can be left floating if not used. PG can be used to drive power-on reset circuitry or used as a low-battery indicator.

Regulator Protection

The TS6112-33 PMOS-pass transistor has a built-in back diode that conducts reverse currents when the input Voltage drops below the output voltage (e.g., during power down). Current is conducted from the output to the Input and is not internally limited. When extended reverse voltage is anticipated, external limiting may be appropriate.

The TS6112-33 also features internal current limiting and thermal protection. During normal operation, the TS6112-33 limits output current to approximately 0.78A (typ). When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, care should be taken not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds +150°C (typ), thermal-protection circuitry shuts it down. Once the device has cooled below +130°C (typ), regulator operation resumes.

Power Dissipation and Junction Temperature

Specified regulator operation is assured to a junction temperature up to +125˚C; the maximum junction temperature should be restricted to +125˚C under normal operating conditions. This restriction limits the power dissipation the regulator can handle in any given application. To ensure that the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using the following equation:

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}}$$

Where:

$T_J$max is the maximum allowable junction temperature.

$R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, i.e., 176°C/W for the SOP8 package.

T_A is the ambient temperature.

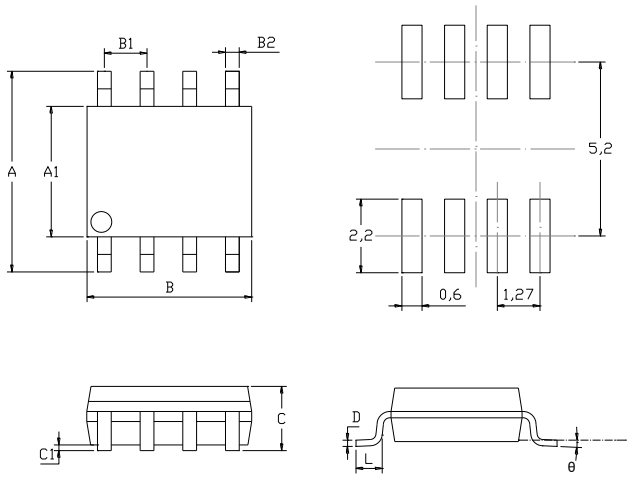
The regulator dissipation is calculated using:

$$P_{D(max)} = (V_{IN} - V_{OUT}) \times I_{OUT}$$

Power dissipation resulting from quiescent current is negligible. Excessive power dissipation will trigger the thermal protection circuit.

MECHANICAL DIMENSIONS

SOP8 PACKAGE MECHANICAL DRAWING

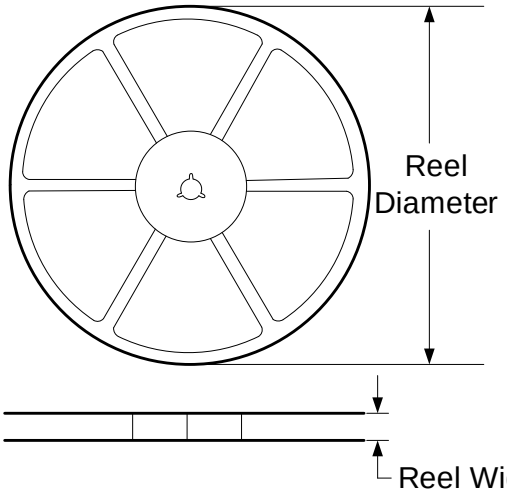


SOP8 PACKAGE MECHANICAL DATA

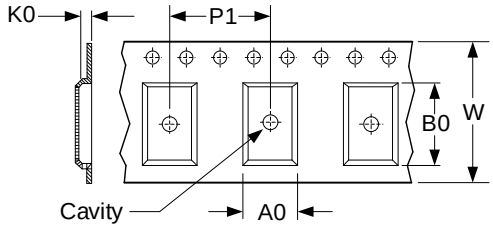
symbol	dimensions			
	millimeters		inches	
	min	max	min	max
A	5.800	6.200	0.228	0.244
A1	3.800	4.000	0.150	0.157
B	4.700	5.100	0.185	0.201
B1	1.270		0.050	
B2	0.330	0.510	0.013	0.020
C		1.750		0.069
C1	0.100	0.250	0.004	0.010
L	0.400	1.270	0.016	0.050
D	0.170	0.250	0.007	0.010
θ	0°	8°	0°	8°

TAPE AND REEL INFORMATION

REEL DIMENSIONS

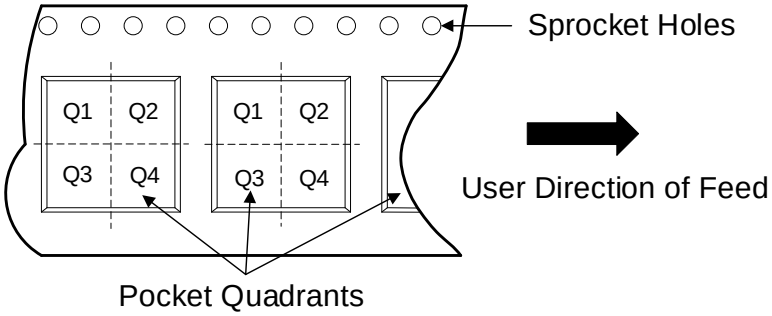


TAPE DIMENSIONS



A0	Dimensioon designed to accommodate the component width
B0	Dimensioon designed to accommodate the component length
K0	Dimensioon designed to accommodate the component width thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS611233SOP8R	SOP8	8	2500	330.0	12.4	6.4	5.4	2.1	8.0	12.0	Q1

REVISION HIETORY

2020/8/7— REV KY1.0.8B TO REV KY1.0.9B

Updated Figure10 7

Updated MECHANICAL DIMENSIONS 11

CONTACT INFORMATION

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