Single-Channel Low-Side Driver IC with OCP

FEATURES

- **Over-current detection with negative voltage input**
- **Over-current threshold accuracy at 25℃: ±6%(±15mV)**
- **Single pin for fault output and enable**
- **Programmable fault clear time**
- **Under voltage lockout for IGBTs**
- **CMOS Schmitt-triggered inputs**
- **3.3V, 5V and 15V input logic compatible**
- **20V V_{CC} voltage supply support (max)**
- **Output in phase with input**
- **Leadfree, RoHS Compliant**

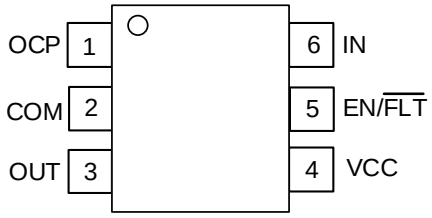
APPLICATIONS

- **Digitally controlled PFC**
- **Home appliances**
- **Air conditioner**
- **Industrial applications**
- **General purpose low-side gate driver for single-ended topologies**

PRODUCT DESCRIPTION

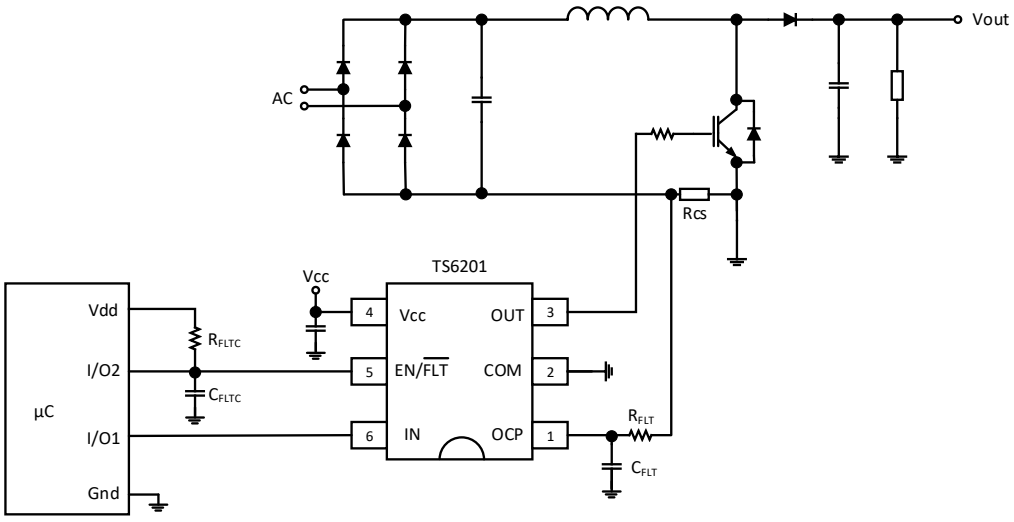
The TS6201 is a low-voltage, power IGBT, non-inverting gate driver. The logic input is compatible with standard CMOS or LSTTL output. The TS6201 has OCP pin for over current protection sense and a FAULT status output (when activivated, EN/FLT pin is internally pulled down). The EN/FLT needs to be externally pulled up to provide normal operation, pulling EN/FLT low disable the driver. Internal circuitry on VCC pin provides an under voltage lockout protection that holds output low until Vcc supply voltage is within operating range.

PIN ASSIGNMENTS



SOT-23-6L

TYPICAL APPLICATION



ORDERING INFORMATION

Model	Part Number	Eco Plan	Package	Container, Pack Qty
TS6201	TS6201SOT236L	RoHS	SOT-23-6L	Reel, 3000

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted) (1)

Parameter	Min	Max	Unit
Supply Voltage	-0.3	25	V
Input Voltage	-10	V_{CC}+0.3	V
Output Voltage	-0.3	V_{CC}+0.3	V
Voltage at current sense pin (OCP)	-10	V_{CC}+0.3	V
Voltage at enable and fault reporting pin (EN/FLT)	-0.3	V_{CC}+0.3	V
Junction Temperature	-40	150	˚C
Storage Temperature Range	-65	150	˚C
Lead Temperature (Soldering, 10s)		260	˚C
ESD HBM	±6000V		
ESD MM	±600V		
ESC CDM	±1500V		
IC Latch-Up Test at Room Temperature	±600mA @25℃		

(1) Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

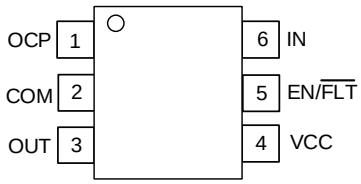
RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Max	Unit
Supply Voltage	12	20	V
Input Voltage	-5	V_{CC}	V
Output Voltage	COM	V_{CC}	V
Voltage at current sense pin (OCP)	-5	V_{CC}	V
Voltage at enable and fault reporting pin (EN/FLT)	0	V_{CC}	V
Ambient temperature	-40	125	℃

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjects to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION

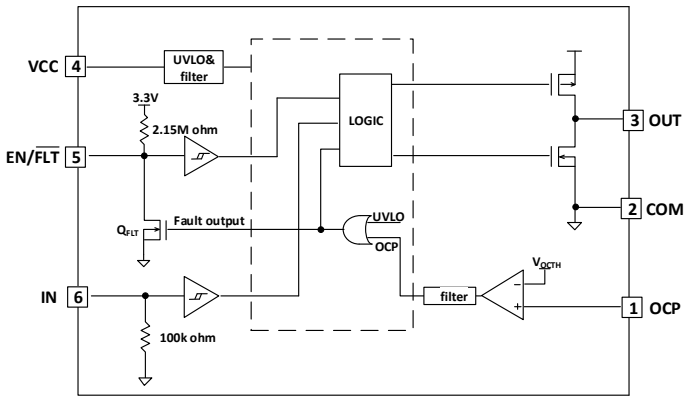


Pin No	Symbol	Function
1	OCP	Current sense input
2	COM	Ground
3	OUT	Gate drive output
4	VCC	Supply Voltage
5	EN/ $\overline{\text{FLT}}$	Enable, fault reporting and fault clear time program pin, three functions: 1. Logic input to enable I/O functionality. I/O logic functions when ENABLE is high. 2. Fault reporting function like over-current or undervoltage lockout, this pin has negative logic and an open-drain output. 3. Fault clear time program with external resistor and capacitor.
6	IN	Logic input for gate driver output (OUT), in phase

INPUT/OUTPUT LOGIC TRUTH TABLE

IN	UVLO	OCP	EN/FLT	OUT	Note
L	H	L	H	L	OUT=L
H	H	L	H	H	OUT=H
X	L	X	L	L	OUT = L, EN/FLT = L, (UVLO protection will disable input signals until EN/FLT returns to high level.)
X	H	H	L	L	OUT = L, EN/FLT = L, (Over current protection will disable input signals until EN/FLT returns to high level.)
X	H	X	L	L	OUT = L (Externally pull down EN/FLT pin will disable I/O logic until EN/FLT returns to high level.)

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

At T_A = +25℃, C_L = 1 nF and V_{CC} = 15V (unless otherwise noted)

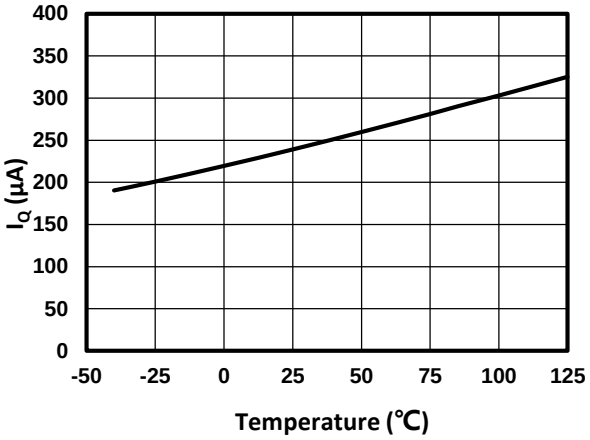
Parameter		Operating Conditions	Min	Typ	Max	Unit
Power Supply						
I_Q	Quiescent Supply Current	V_{IN} = 0V/5V,V_{OCP} = 0V,$V_{EN/FLT}$ = NC,V_{OUT} = NC		240	400	μA
V_{CC_Clamp}	V_{CC} Zener Clamp Voltage (2)	I_Q = 1mA		27		V
V_{UVLO+}	V_{CC} undervoltage Lockout Exit		10.7	11.4	12.2	V
V_{UVLO-}	V_{CC} undervoltage Lockout Enter		9.8	10.5	11.3	V
$V_{UVLO\ HYST}$	V_{CC} undervoltage lockout hysteresis			0.9		V
Input Characteristics						
V_{INH}	Logic “1” Input Voltage		2.5			V
V_{INL}	Logic “0” Input Voltage				0.8	V
I_{INH}	Logic “1” Input Current	V_{IN} = 5V	30	50	70	uA
I_{INL}	Logic “0” Input Current	V_{IN} = 0V		0		uA
V_{ENH}	Logic “1” enable voltage		2.5			V
V_{ENL}	Logic “0” disable voltage				0.8	V
V_{OCPTH}	Current limit threshold voltage		-265	-250	-235	mV
Output Characteristics						
V_{OH}	High level output voltage, V_{CC} -V_{OUT}	I_{OUT} = 2mA		10	100	mV
V_{OL}	Low level output voltage, V_{OUT}	I_{OUT} = -2mA		10	100	mV
I_{O+}	Output sourcing short circuit pulsed current (2)	V_{IN} = 5V,V_{OUT}=0V(Pulse Width≤2 μs)		1.5		A
I_{O-}	Output sinking short circuit pulsed current (2)	V_{IN} = 0V,V_{OUT}=15V(Pulse Width≤2 μs)		1.5		A
I_{FLT}	EN/FLT pull down sinking current	$V_{EN/FLT}$=0.4V	10			mA
V_{ACTSD}	Active shut down voltage	V_{CC}=NC,I_{OUT}=I_{O-}*0.1(150mA)		3.5		V
Time Characteristics						
t_{on}	Turn-on propagation delay	V_{IN} pulse=5V(t_r<5ns, t_f<5ns)		40	70	ns
t_{off}	Turn-off propagation delay			40	70	ns
t_r	Output rise time			10	20	ns
t_f	Output fall time			10	20	ns
t_{DISA}	Disable propagation delay	$V_{EN/FLT}$ pulse=5V		50	75	ns
t_{OCPDEL}	Over current protection propagation delay	V_{OCP} pulse = -0.5V		260	350	ns
t_{OCPFLT}	OCP to low level EN/FLT signal delay	$R_{EN/FLT}$=10kΩ to 3.3V,V_{OCP} pulse = -0.5V		230	320	ns
t_{FLTC}	FAULT clear time	$R_{EN/FLT}$=1MΩ to 3.3V,$C_{EN/FLT}$=150pF to COM	80	103	130	μs
t_{BLK}	Over current protection blanking time (2)	V_{OCP} pulse = -0.5V		120		ns
tv_{CCUV}	V_{CC} supply UVLO filter time (2)			2.4		us

(2) Parameter verified by design, not tested in production.

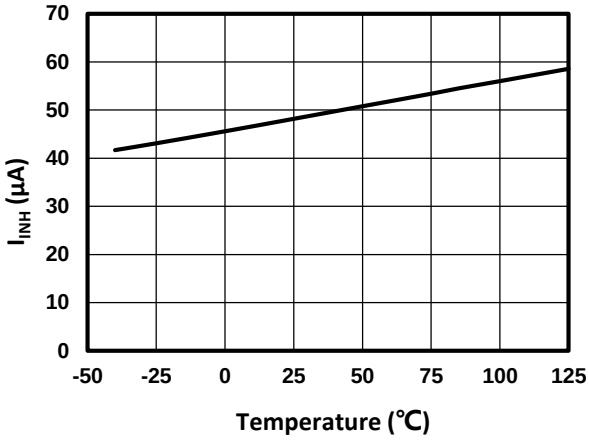
TYPICAL CHARACTERISTICS

At T_A = +25℃, C_L = 1 nF and V_{CC} = 15V (unless otherwise noted)

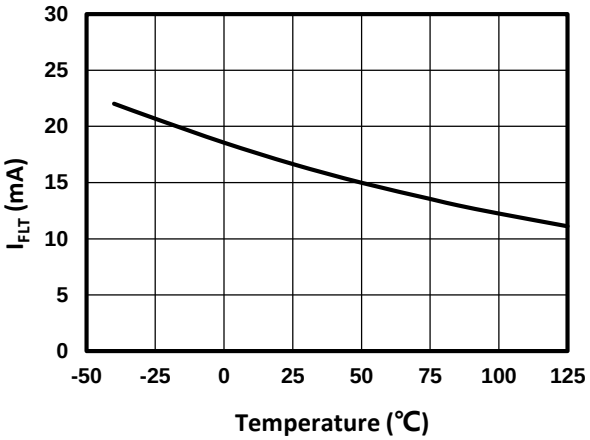
I_Q vs Temperature



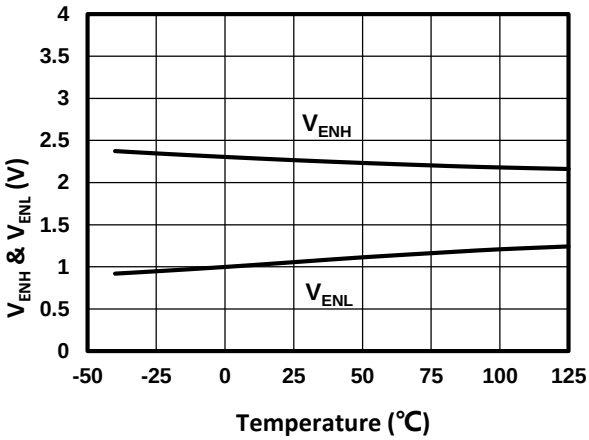
I_{INH} vs Temperature



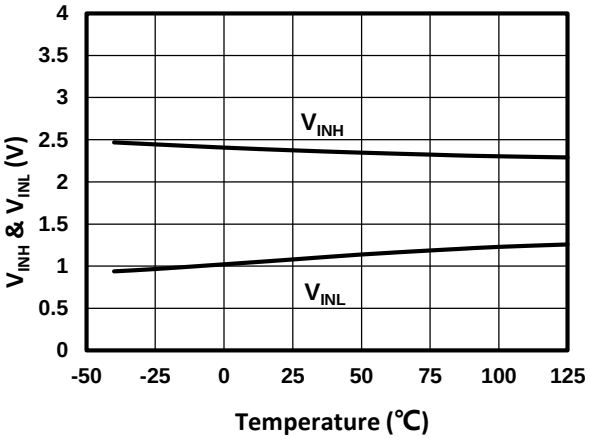
I_{FLT} vs Temperature



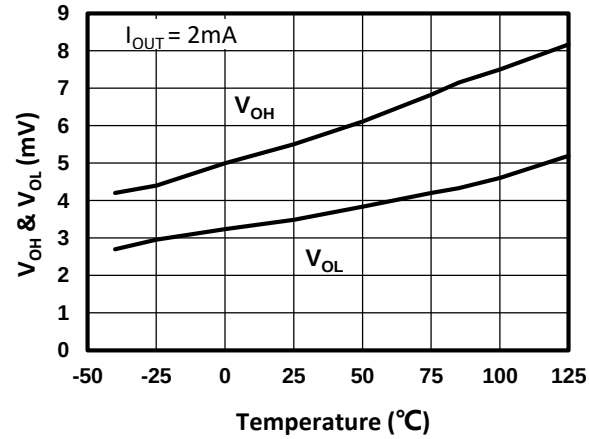
V_{ENH} & V_{ENL} vs Temperature



V_{INH} & V_{INL} vs Temperature



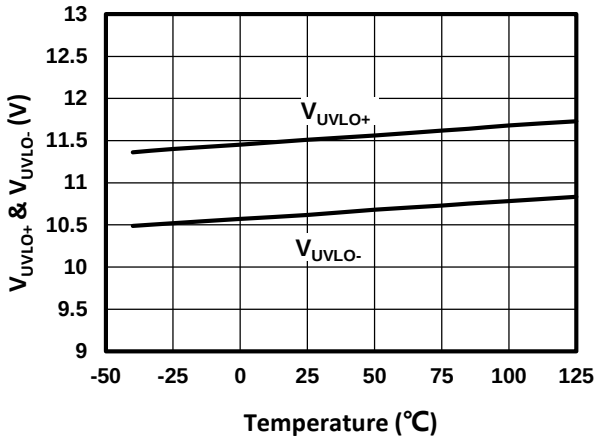
V_{OH} & V_{OL} vs Temperature



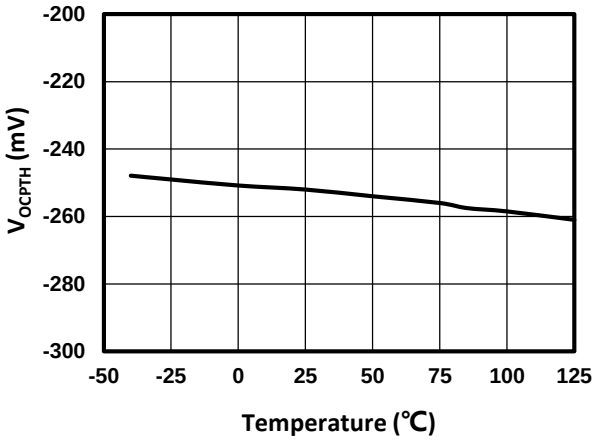
TYPICAL CHARACTERISTICS (CONTINUE)

At T_A = +25℃, C_L = 1 nF and V_{CC} = 15V (unless otherwise noted)

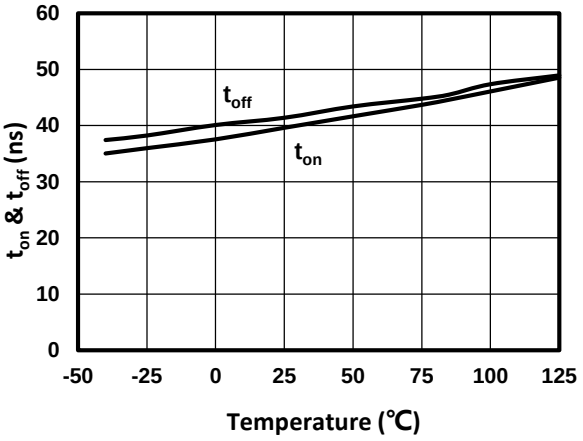
V_{UVLO+} & V_{UVLO-} vs Temperature



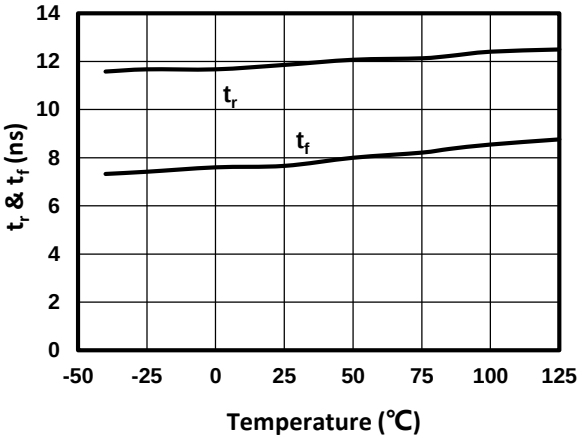
V_{OCPTH} vs Temperature



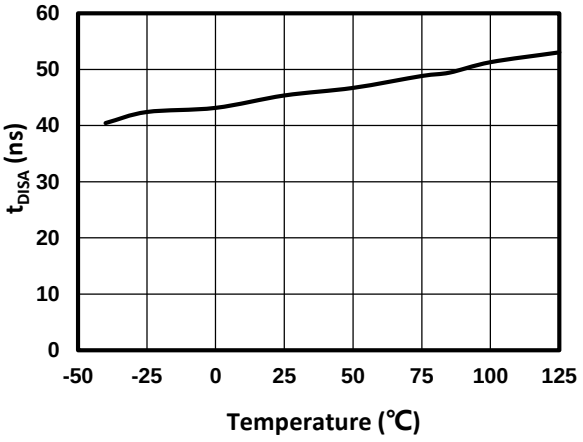
t_{on} & t_{off} vs Temperature



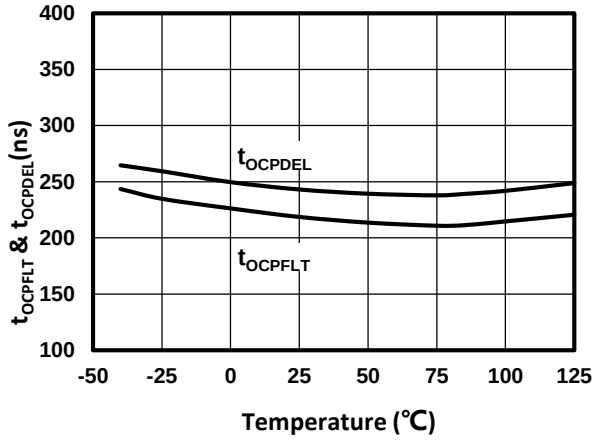
t_r & t_f vs Temperature



t_{DISA} vs Temperature



t_{OCPFLT} & t_{OCPDEL} vs Temperature



APPLICATION NOTES & ADDITIONAL DETAILS

Switching and Timing Relationships

The relationship between the input and output of the product is shown in Figure 1. It is also shown on the figure the definition of timing parameters including t_{on}, t_{off}, t_r, and t_f.

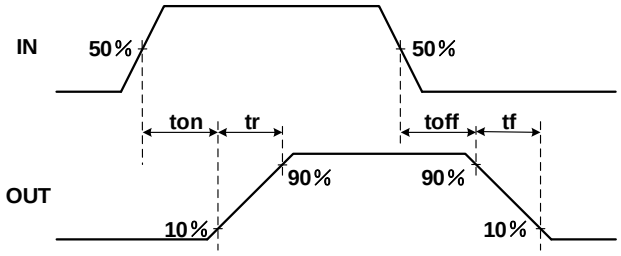


Figure 1. Switching Time Waveform Definitions

The test circuit for the timing parameters is shown in Figure 2. The capacitor on the power supply should be placed as close as possible to the power pin, to prevent the power supply voltage from being pulled down during output switching.

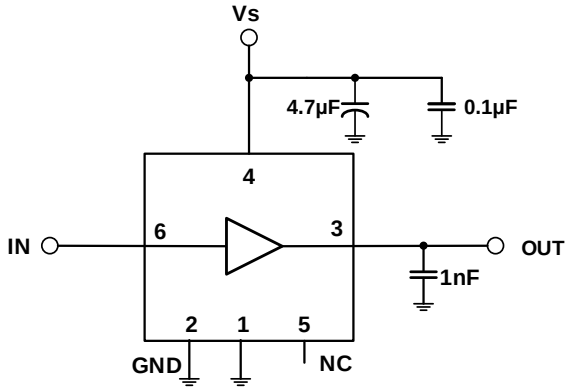


Figure 2. Test Circuit for Switching Time

Input Logic Compatibility

The input voltage of this product is compatible with TTL and CMOS levels. Input hysteresis offers enhanced noise immunity. The built-in 100k ohm pull-down resistor puts the output low when the input pin is floating. Figure 3 illustrates the relationship between input voltage and input logic.

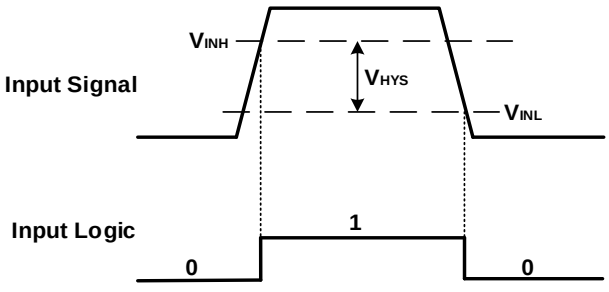


Figure 3. Input Logic and Input Threshold Voltages

APPLICATION NOTES & ADDITIONAL DETAILS(CONTINUE)

● Undervoltage Lockout

The product has a built-in UVLO function. When the power supply voltage is lower than V_{UVLO-}, the output will remain low regardless of the input state. When the power supply voltage exceeds the V_{UVLO+}, the output pin will continue to maintain the low level, and the output will not change with the input until the input pin has a rising edge. Figure 4 shows the above function.

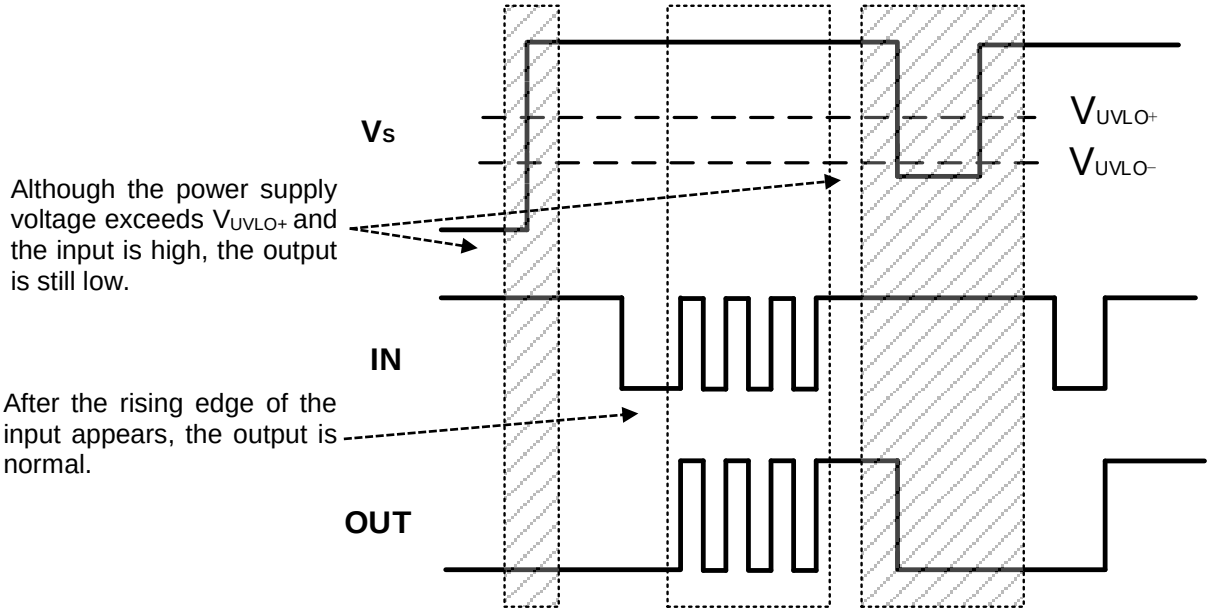


Figure 4. Vs Under Voltage Protection Waveform Definitions

The circuit includes a deglitch filter with about 2μs delay that can effectively avoid mis-trigger events. Figure 6 shows the implementation principle of the internal filter circuit.

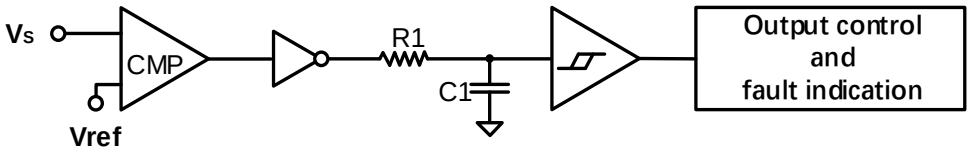


Figure 5. Block Diagram of UVLO Filter Circuit

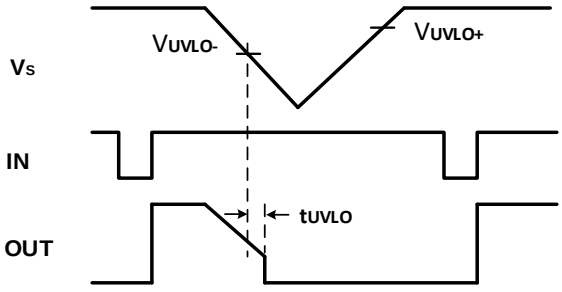


Figure 6. Delay Time of UVLO Filter

APPLICATION NOTES & ADDITIONAL DETAILS(CONTINUE)

● V_S Voltage Clamp

The internal power supply pin V_S of the product is integrated with a voltage clamping function, which can protect the power transistor inside the chip in case of transient overvoltage on the power supply. Figure 7 shows the output waveforms with and without this function.

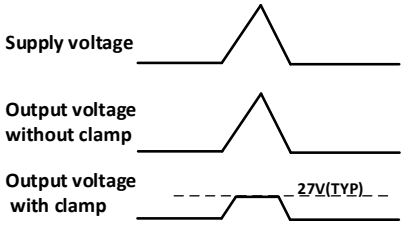


Figure 7. Output Waveform with and without Clamping

● Active Shutdown

The active shutdown function is a protection feature of the driver. It is designed to avoid a free floating gate of a connected power switch to false trigger a turn on. In case of supply voltage failure at the V_S pin, the output section of the driver operates in the active shutdown mode. In this case the driver uses the floating voltage of the connected gate to supply this internal circuit. This solution is by far stronger than an otherwise used R_{GS}.

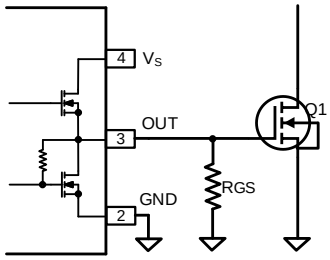


Figure 8. Block Diagram of Active Shutdown Circuit

● Typical Application of PFC

Figure 9 shows the typical application of TS6201 when used as a gate driver for the power MOSFET in a boost-converter application (for example, AC-DC power factor correction in offline chargers for electric vehicles). Since the output pin of the product is integrated with the *Active Shut Down* function, and the power transistor will remain off when power is cut off. Thus, the pull-down resistor in the figure is optional.

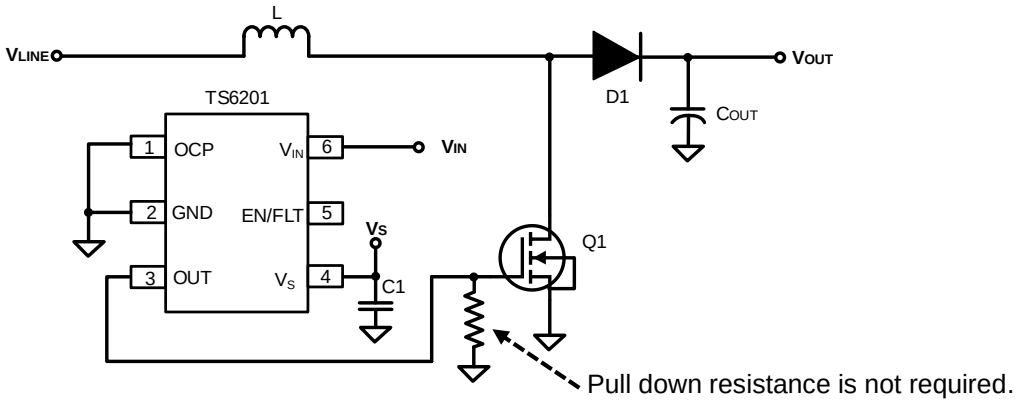


Figure 9. Typical Application in PFC Power Stage Without OCP and EN/FLT

Over current protection (OCP)

The TS6201 has a function of over current protection with a threshold V_{OCPTH} at the OCP pin input. The voltage at this pin is the negative voltage drop sensed across the system current sense resistor. It is up to minus 10 V_{DC} negative input capability of OCP pin. To avoid false tripping due to the fast high current switch on transient that occurs at the switch on of IGBT resulting from the circuit parasitic capacitors, there is a blanking interval which disables over current detection for the period of t_{BLK} (Additional RC filter is recommended, if internal t_{BLK} is not enough in the very noisy circuit.). After t_{BLK} and the voltage of OCP pin is over V_{OCPTH}, the TS6201 causes fault logic to initiate a fault shutdown sequence. This sequence starts with the generation of a fault signal and internal MOSFET Q_{FLT} is turned on and EN/FLT pin is pulled down.

At the same time the TS6201 terminates the present cycle, and the gate output is immediately pulled down with internal propagation delay (t_{OCPDEL}), see the Figure 10 and Figure 11.

Figure 9 is the diagram of TS6201 in boost application. And Figure 10 is the typical waveforms of the application. If the OCP fault condition is removed, the internal pull down NMOS of EN/FLT is released and EN/FLT will be pull up again with V_{dd}, but the output still keeps low until the next input signal IN is high.

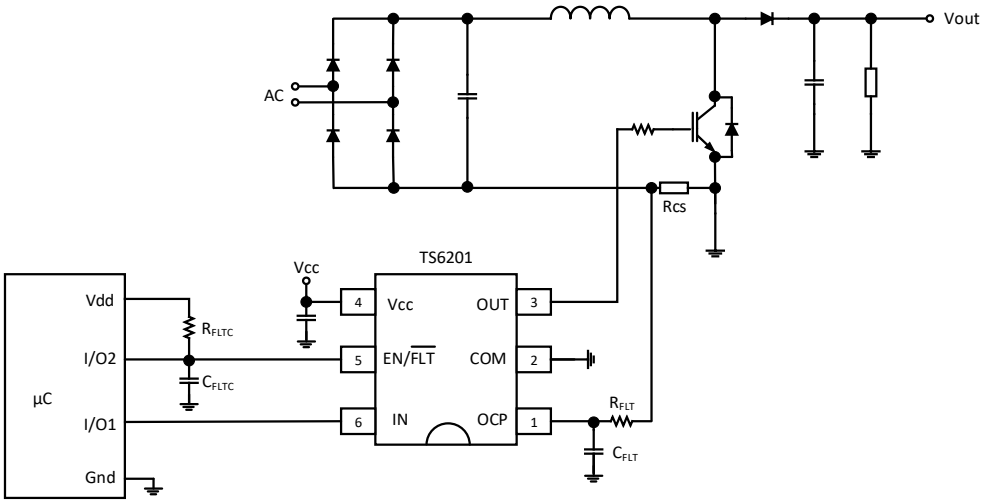


Figure 10. TS6201 in Boost Application

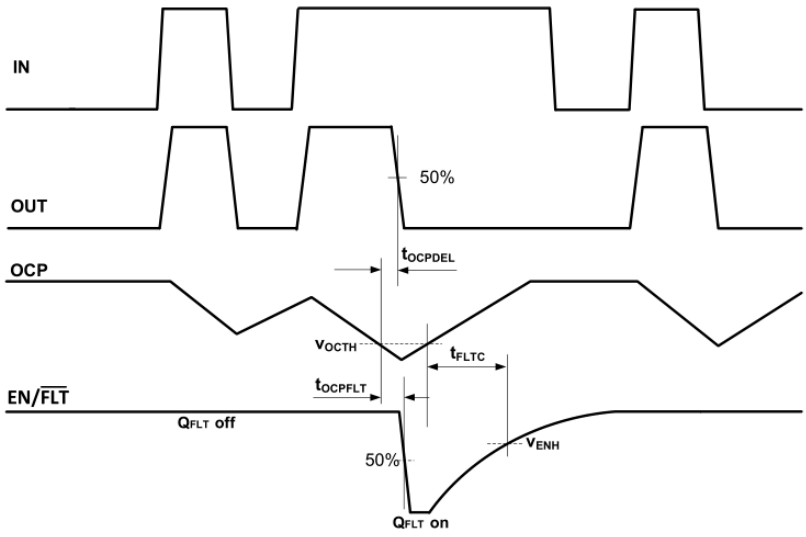


Figure 11. OCP Fault Detection and Fault Clear Waveforms One

Fault reporting and programmable fault clear timer

The TS6201 provides an integrated fault reporting output and an adjustable fault clear timer. There are two situations that would cause the driver to report a fault via the EN/FLT pin. The first is an under voltage condition of V_{CC} and the second is if the OCP pin recognizes a fault. Once the fault condition occurs, the EN/FLT pin is internally pulled to COM. The EN/FLT output stays in the low state until the fault condition has been removed and the internal pull down NMOS Q_{FLT} turns off, the voltage on the EN/FLT pin is charged up with external pull-up voltage.

The length of the fault clear time period (t_{FLTC}) is determined by exponential charging characteristics of the capacitor where the time constant is set by R_{FLTC} and C_{FLTC}. Figure 10 shows that R_{FLTC} is connected between the external supply (V_{DD}) and the EN/FLT pin, while C_{FLTC} is placed between the EN/FLT and COM pins. EN/FLT is weakly pulled up to 3.3 V reference voltage with 2.15M resistor internally. So the length of the fault clear time period can be determined by using the formula below (If V_{DD} = 3.3 V).

$$t_{FLTC} = -\left(\frac{R_{FLTC} \times 2.15M}{R_{FLTC} + 2.15M}\right) \times C_{FLTC} \times \ln\left(1 - \frac{V_{ENH}}{V_{DD}}\right)$$

Enable input

TS6201 provides an enable functionality that allows to shutdown or to enable the output. When EN/FLT is pulled up (the enable voltage is higher than V_{ENH}) the output is able to operate normally, pulling EN/FLT low (the enable voltage is lower than V_{ENL}) the output is disable. The relationships between the input, output and enable signals of the TS6201 are illustrated below in Figure 12~14. From these figures, we can see the definitions of several timing parameters and threshold voltages (i.e. t_{DISA}, V_{ENH} and V_{ENL}) associated with this device.

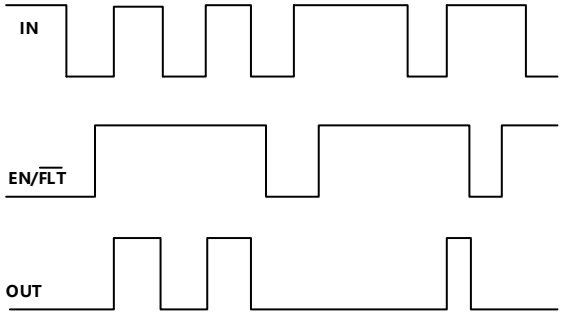


Figure 12. Input/Output/Enable Pins Timing Diagram

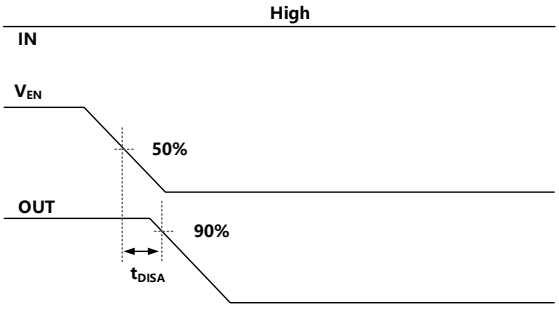


Figure 13. EN Pin Switching Time Waveform

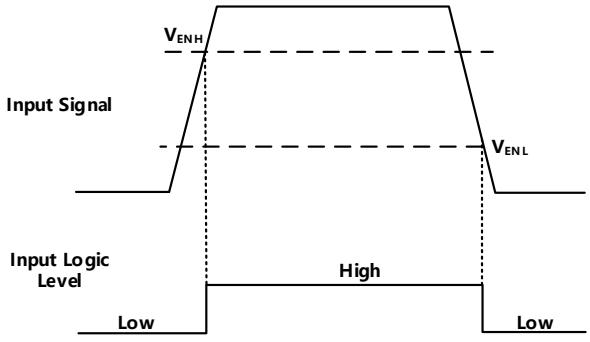
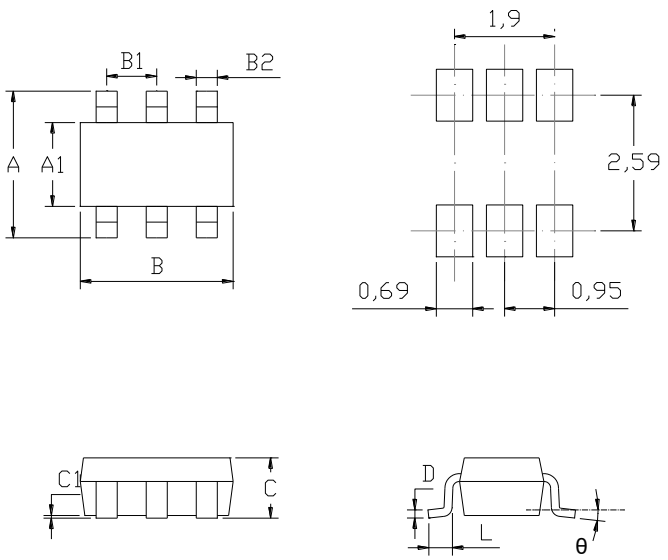


Figure 14. EN Input Thresholds

MECHANICAL DIMENSIONS

SOT-23-6L PACKAGE MECHANICAL DRAWING

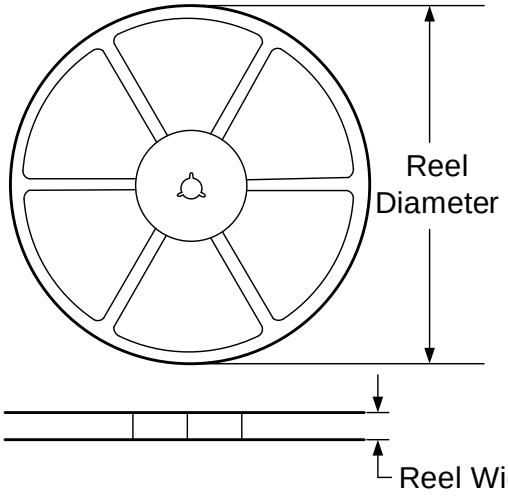


SOT-23-6L PACKAGE MECHANICAL DATA

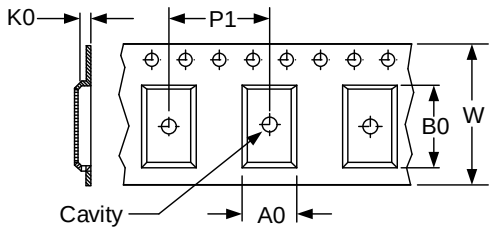
symbol	dimensions			
	millimeters		inches	
	min	max	min	max
A	2.65	2.95	0.104	0.116
A1	1. 50	1.70	0.059	0.067
B	2.82	3.02	0.111	0.119
B1	0.95		0.037	
B2	0.30	0.50	0.012	0.020
C		1.25		0.049
C1	0.00	0.10	0.000	0.004
L	0.30	0.60	0.012	0.024
D	0.10	0.20	0.004	0.008
θ	0º	8º	0º	8º

TAPE AND REEL INFORMATION

REEL DIMENSIONS

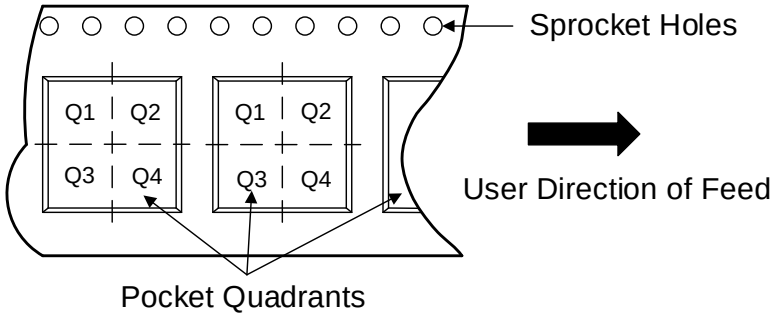


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component width thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TS6201SOT236L	SOT-23-6L	6	3000	180.0	9.0	3.2	3.3	1.4	4.0	8.0	Q3

REVISION HISTORY

NOTE: Page numbers for previous revisions may be different from that of the current version.

2023/12/22— REV KY0.0.0 TO REV KY1.0.0

Update parameters related to OCP ……all pages

2024/05/21— REV KY1.0.0 TO REV KY1.1.0

Delete **A Grade** ……1、2、4、13

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