High Speed Single Low Side Driver

FEATURES

- **Rail-to-Rail Output**
- **Under voltage lockout**
- **1.5A Peak Output Current**
- **Wide Operating Range: 12V to 20V**
- **Input Voltages up to V_S**
- **3.3 V, 5 V and 15 V input logic compatible**
- **Short Delay Time: 45ns at V_S = 15V**
- **Output Rise and Fall Time of 10ns with 1000pF Load at V_S = 15V**
- **Low Supply Current: 200μA at V_S = 15V**
- **Leadfree, RoHS Compliant**

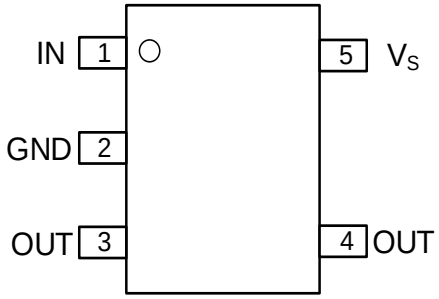
PRODUCT DESCRIPTION

The TS62373 is a single channel, high speed power MOSFET and IGBT driver, which is designed for applications that require low current signals to drive large capacitive loads with high speed. The input current is very low so that it is compatible with standard CMOS or LSTTL output. The output drivers feature a high pulse current buffer stage designed for minimum rise and fall time. Excellent latch immune performance is achieved.

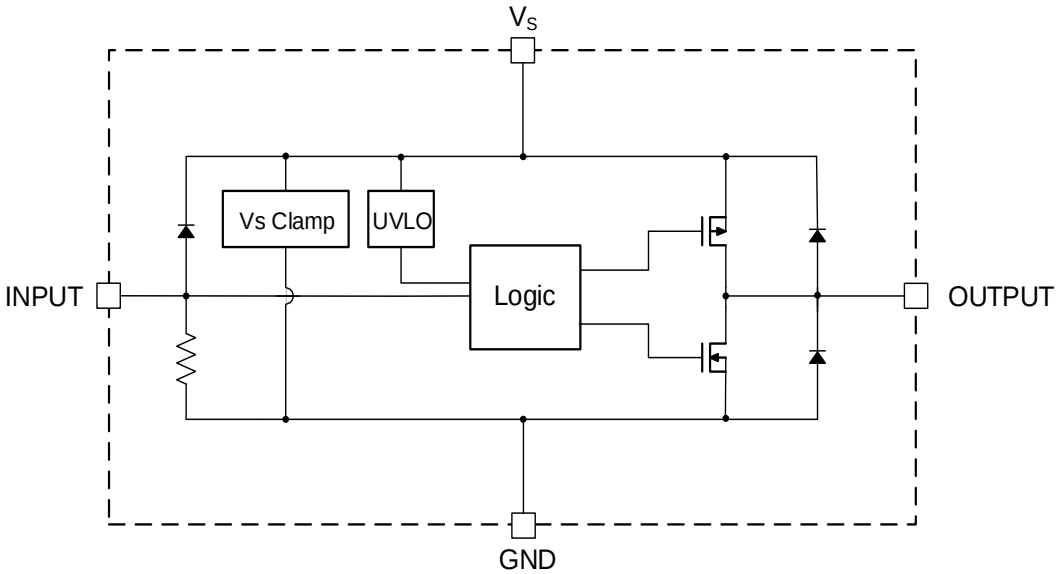
APPLICATIONS

- **Switching Mode Power Supplies**
- **Motor Drivers**
- **General Purpose Single Low Side Drivers**

PIN CONFIGURATION



BLOCK DIAGRAM



ORDERING INFORMATION

Product	Part Number	MSL	Eco Plan	Package	Container, Pack Qty
TS62373	TS62373SOT235R	MSL2	RoHS	SOT-23-5L	Reel, 3000

RECOMMENDED OPERATING CONDITIONS

Parameter	Min	Max	Unit
Vs to GND Voltage	12	20	V
Input Voltage(Figure 6)	-5	V_S	V
Operating Temperature	-40	125	˚C

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted) (1)

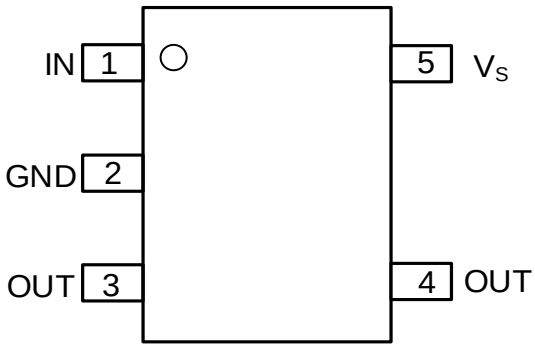
Parameter	Min	Max	Unit
V_S to GND Voltage	-0.3	25	V
Input Voltage	-10	V_S + 0.3	V
Output Voltage	- 0.3	V_S + 0.3	V
Package Power Dissipation @ $T_A \leq 50$˚C		120	mW
Thermal Resistance, Junction to Ambient		191	˚C/W
Junction Temperature	-40	150	˚C
Storage Temperature	-55	150	˚C
Lead Temperature (Soldering, 10s)		300	˚C
ESD HBM	±4kV		
ESD MM	±400V		
ESD CDM	±1500V		
IC Latch-Up Test	±800mA @25˚C		

(1) Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (Electrostatic Discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjects to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION



SOT-23-5L

PIN DEFINITIONS

Pin No.	Symbol	Function
1	IN	Input (with 100kΩ pull-down resistor)
2	GND	Ground
3	OUT	Output
4	OUT	Output
5	V_S	Power Supply

FUNCTION TABLE

UVLO	Input	Output
H	L	L
H	H	H
L	X	L
L->H(2)	H	L
L->H(2)	L	L
L->H(2)	L->H	H

(2) The product has a fault locking function. When the chip switches from UVLO-L state to UVLO-H state, the input terminal needs a rising edge to output high level. This phenomenon mainly occurs during power on. If the input terminal is at a high level before power on, the output terminal will remain at a low level after power on due to the protection function, and the output terminal stays low until the input terminal changes from low to high. In application, a capacitor of at least 0.1uF should be placed as close as possible to the power supply pin of the chip to prevent the power supply voltage from dropping below UVLO-L when the output level switches normally from low to high.

ELECTRICAL CHARACTERISTICS

At T_A = +25°C, C_{LOAD} = 1nF and V_S = 15V (unless otherwise noted)

Parameter		Operating Conditions	Min	Typ	Max	Unit
Input Characteristics						
V_{IH}	Logic 1 Input Voltage (3)		2.7			V
V_{IL}	Logic 0 Input Voltage (3)				0.8	
I_{IN+}	Logic 1 Input Current	IN = 5V		50	75	μA
I_{IN-}	Logic 0 Input Current	IN = 0V		0		
Output Characteristics						
V_{OH}	High output voltage, V_S -V_{OUT}	I_{OUT} = 2mA	0.025			V
V_{OL}	Low Output Voltage, V_{OUT}	I_{OUT} = -2mA			0.025	V
R_{OH}	Output Resistance High State	I_{OUT} = 100mA		2.9		Ω
R_{OL}	Output Resistance Low State	I_{OUT} = -100mA		1.8		Ω
I_{O+}	Peak Output Current	IN = 5V, OUT = 0V		1.5		A
I_{O-}		IN = 0V, OUT = V_S		1.5		A
V_{ACTSD}	Active shutdown voltage	V_S = NC,I_{OUT} = -50mA		2.5		V
Power Supply						
I_Q	Quiescent Supply Current	V_{IN} = 0V/5V, V_{OUT} = NC		200	400	μA
V_{UVLO+}	V_S undervoltage Lockout Exit			11.4		V
V_{UVLO-}	V_S undervoltage Lockout Enter			10.5		
$V_{UVLO\ HYST}$	V_S undervoltage lockout hysteresis			0.9		
V_{S_Clamp}	V_S Zener Clamp Voltage	I_Q = 1mA		27		
Switching Time Characteristics						
t_{on}	Turn-on Propagation Delay	V_{IN} pulse = 5V (t_r<5ns, t_f<5ns)		45	65	ns
t_{off}	Turn-off Propagation Delay			45	65	
t_r	Output Rise Time			10	20	
t_f	Output Fall Time			10	20	
t_{UVLO}	V_s supply UVLO filter time (4)			2.4		us

(3) This parameter is intended to describe the logic level conditions, not the actual threshold voltage of the product. The actual threshold voltage can refer to Figure 5. It can be seen from the figure that the product also contains hysteresis with a typical value of 1.3V, which will effectively prevent output jitter when the input ripple is large.

(4) Parameter verified by design, not tested in production.

TYPICAL CHARACTERISTICS

At T_A = +25°C, C_{LOAD} = 1nF, and V_S = 15V (unless otherwise noted)

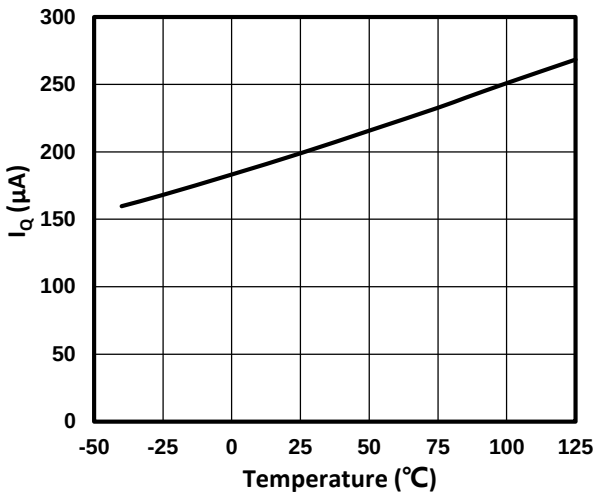


Figure 1. I_Q vs Temperature

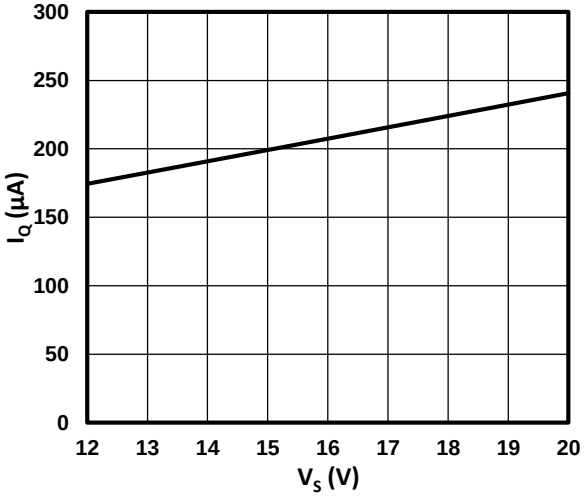


Figure 2. I_Q vs V_S

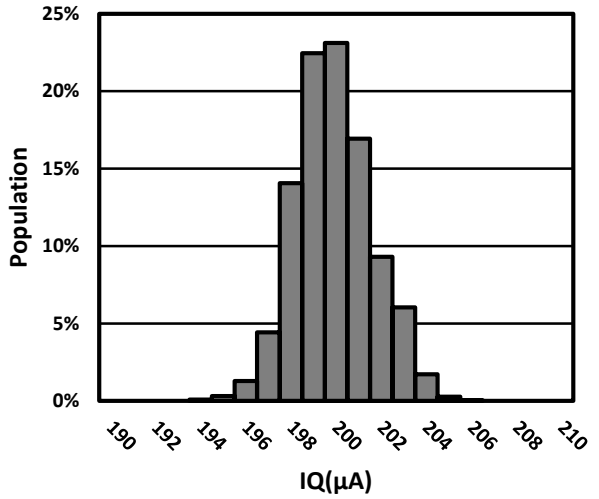


Figure 3. I_Q Production Distribution

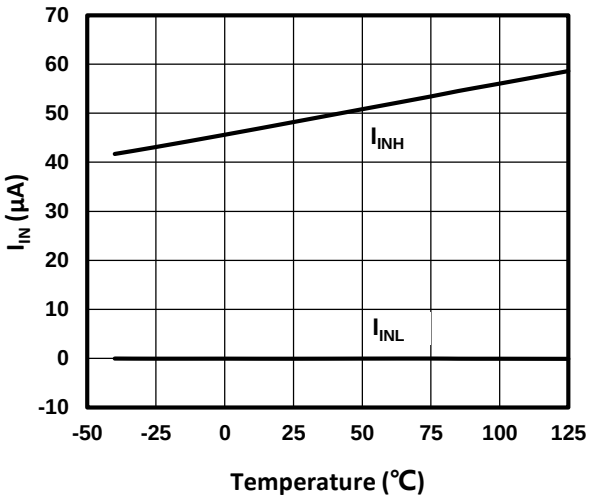


Figure 4. I_{IN} vs Temperature

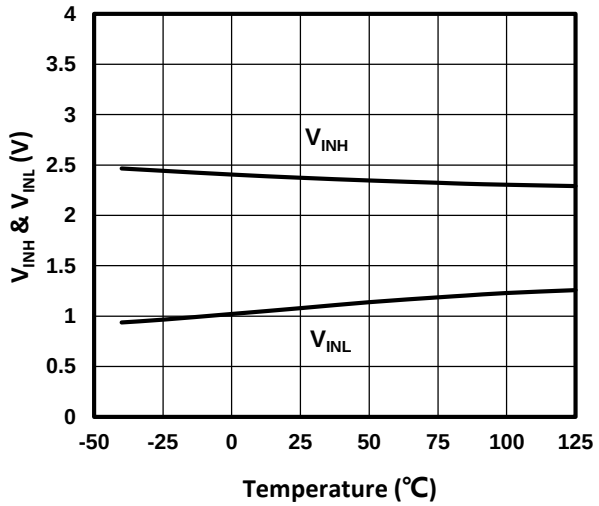


Figure 5. V_{INH} & V_{INL} vs Temperature

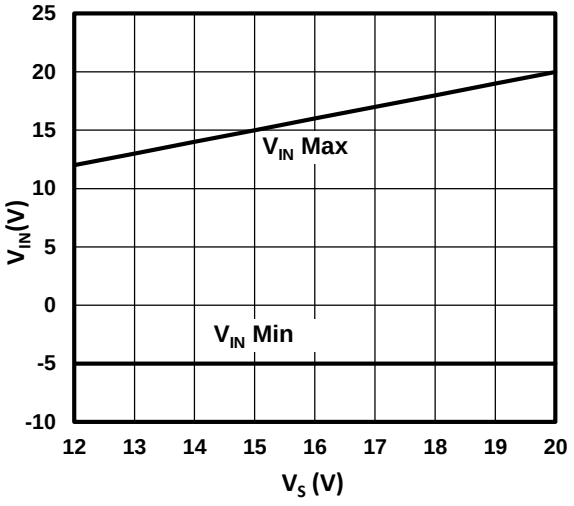


Figure 6. Recommend Input Range vs V_S

TYPICAL CHARACTERISTICS (CONTINUE)

At T_A = +25℃, C_L = 1 nF and Vs = 15V (unless otherwise noted)

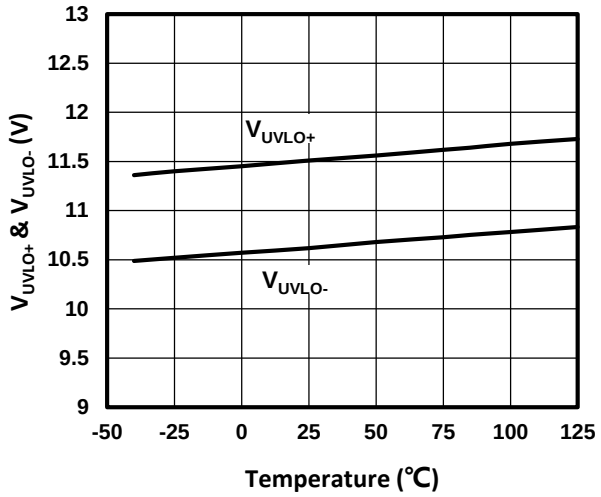


Figure 7. V_{UVLO+} & V_{UVLO-} vs Temperature

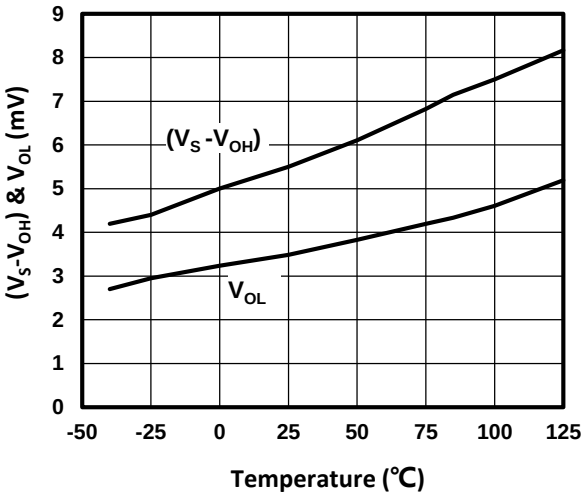


Figure 8. (V_S – V_{OH}) & V_{OL} vs Temperature

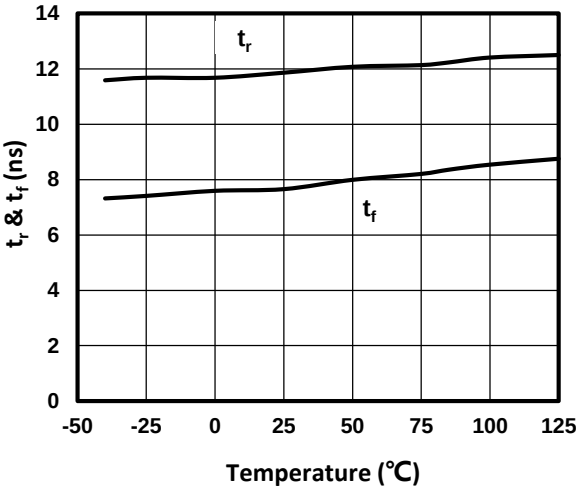


Figure 9. t_r & t_f vs Temperature

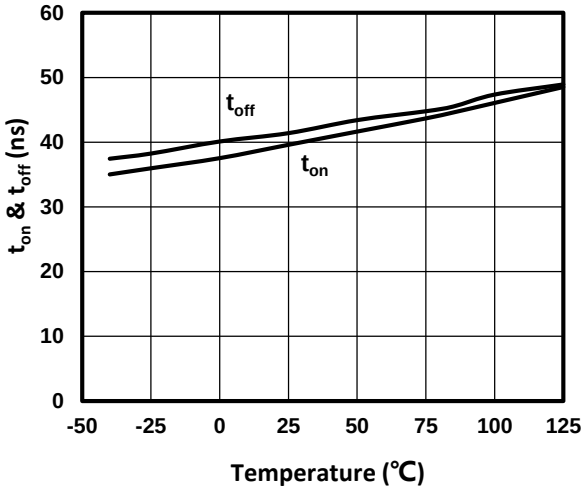


Figure 10. t_{on} & t_{off} vs Temperature

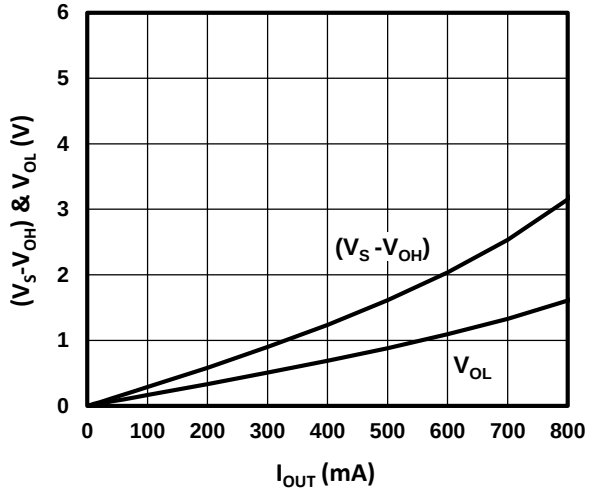


Figure 11. (V_S – V_{OH}) & V_{OL} vs I_{OUT}

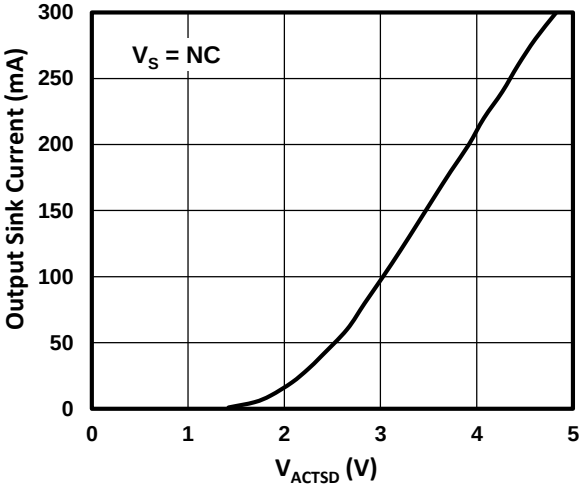


Figure 12. V_{ACTSD} vs Output Sink Current

APPLICATION NOTES & ADDITIONAL DETAILS

Switching and Timing Relationships

The relationship between the input and output of the product is shown in Figure 13. It is also shown on the figure the definition of timing parameters including t_{on}, t_{off}, t_r, and t_f.

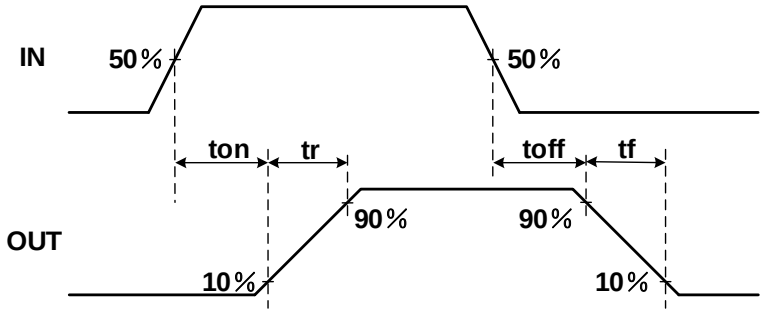


Figure 13. Switching Time Waveform Definitions

The test circuit for the timing parameters is shown in Figure 14. The capacitor on the power supply should be placed as close as possible to the power pin, to prevent the power supply voltage from being pulled down during output switching.

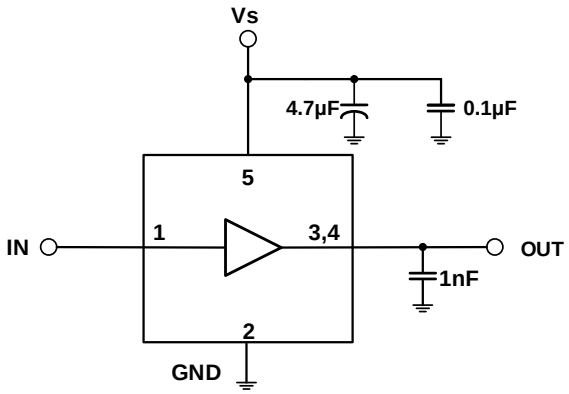


Figure 14. Test Circuit for Switching Time

Input Logic Compatibility

The input voltage of this product is compatible with TTL and CMOS levels. Input hysteresis offers enhanced noise immunity. The built-in 100k ohm pull-down resistor puts the output low when the input pin is floating. Figure 15 illustrates the relationship between input voltage and input logic.

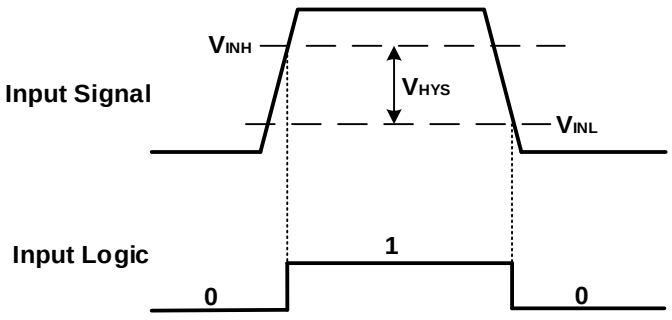


Figure 15. Input Logic and Input Threshold Voltages

APPLICATION NOTES & ADDITIONAL DETAILS(CONTINUE)

● Undervoltage Lockout

The product has a built-in UVLO function. When the power supply voltage is lower than V_{UVLO-}, the output will remain low regardless of the input state. When the power supply voltage exceeds the V_{UVLO+}, the output pin will continue to maintain the low level, and the output will not change with the input until the input pin has a rising edge. Figure 16 shows the above function.

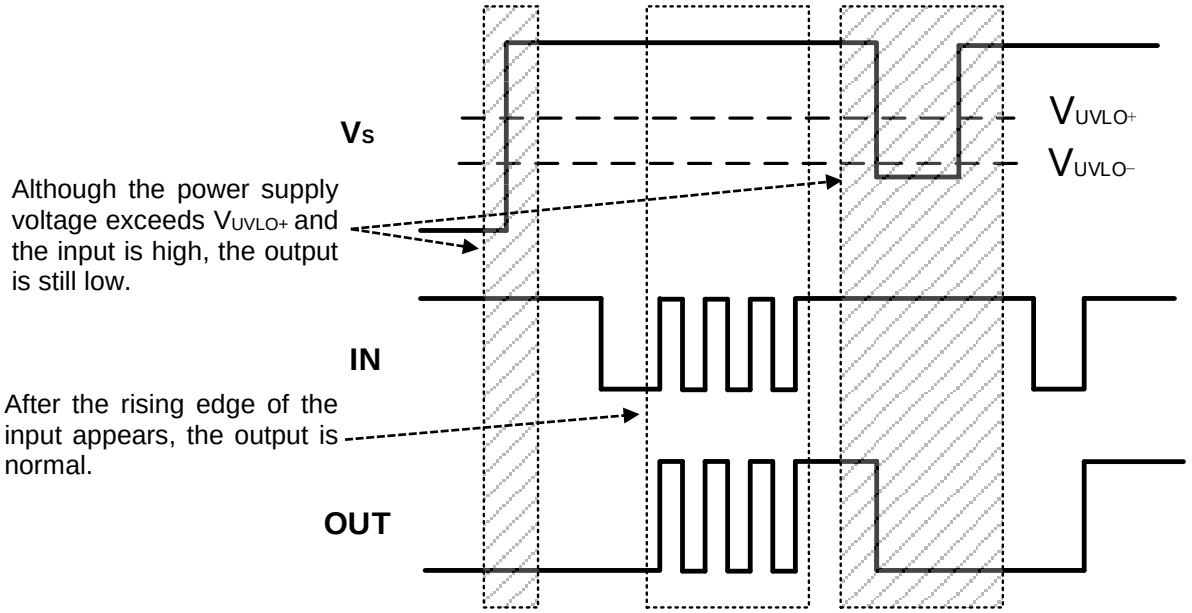


Figure 16. Vs Under Voltage Protection Waveform Definitions

The circuit includes a deglitch filter with about 2μs delay that can effectively avoid mis-trigger events. Figure 17 shows the implementation principle of the internal filter circuit.

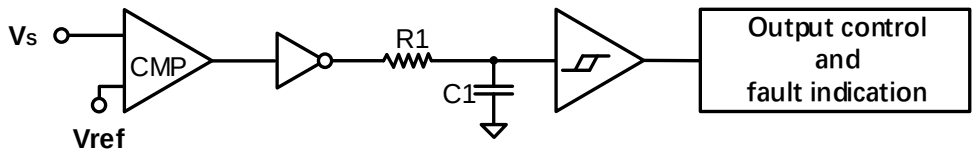


Figure 17. Block Diagram of UVLO Filter Circuit

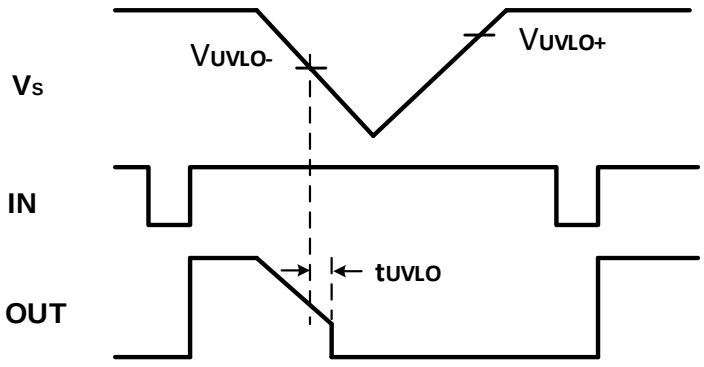


Figure 18. Delay Time of UVLO Filter

APPLICATION NOTES & ADDITIONAL DETAILS(CONTINUE)

• V_S Voltage Clamp

The internal power supply pin V_S of the product is integrated with a voltage clamping function, which can protect the power transistor inside the chip in case of transient overvoltage on the power supply. Figure 19 shows the output waveforms with and without this function.

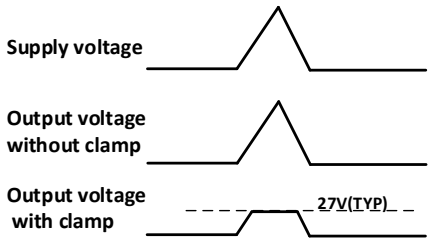


Figure 19. Output Waveform with and without Clamping

• Active Shutdown

The active shutdown function is a protection feature of the driver. It is designed to avoid a free floating gate of a connected power switch to false trigger a turn on. In case of supply voltage failure at the V_S pin, the output section of the driver operates in the active shutdown mode. In this case the driver uses the floating voltage of the connected gate to supply this internal circuit. This solution is by far stronger than an otherwise used R_{GS}.

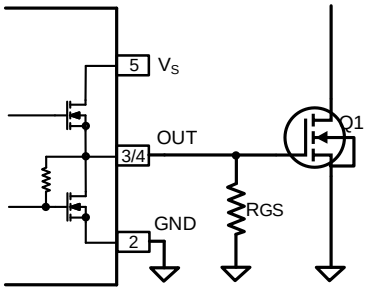


Figure 20. Block Diagram of Active Shutdown Circuit

• Typical Application of PFC

Figure 21 shows the typical application of TS62373 when used as a gate driver for the power MOSFET in a boost-converter application (for example, AC-DC power factor correction in offline chargers for electric vehicles). Since the output pin of the product is integrated with the *Active Shut Down* function, and the power transistor will remain off when power is cut off. Thus, the pull-down resistor in the figure is optional.

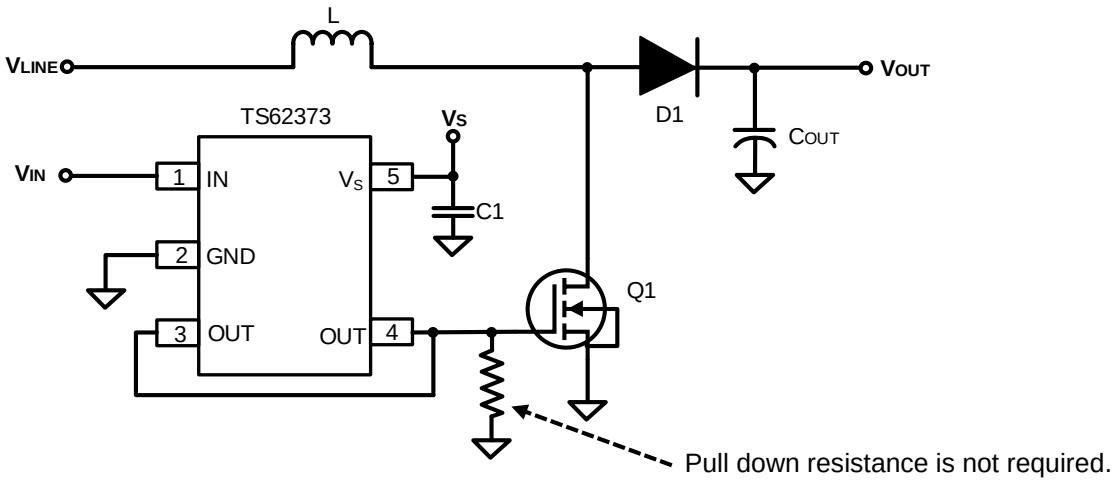
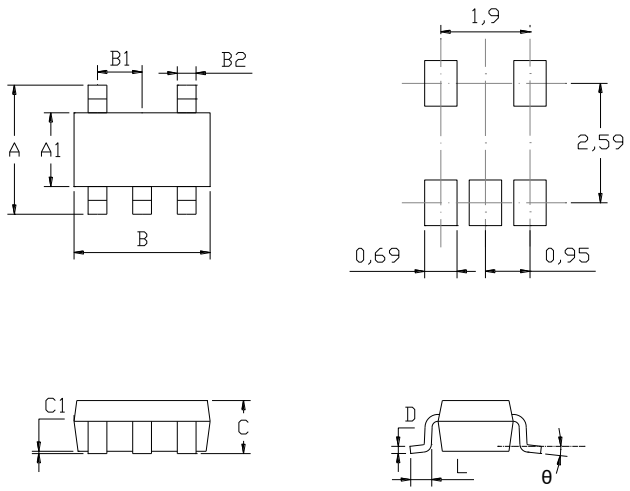


Figure 21. Typical Application in PFC Power Stage

MECHANICAL DIMENSIONS

SOT-23-5L PACKAGE MECHANICAL DRAWING

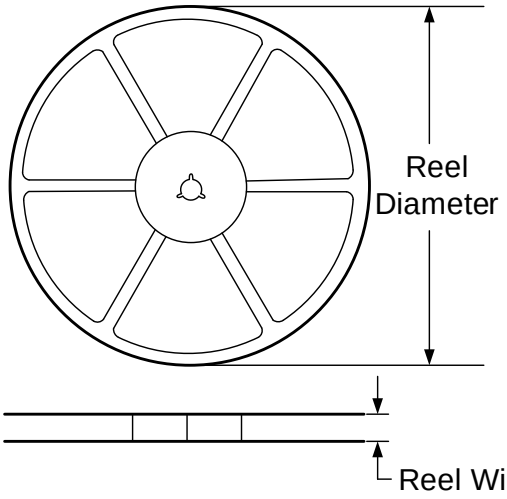


SOT-23-5L PACKAGE MECHANICAL DATA

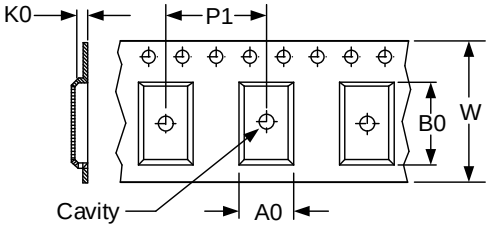
symbol	dimensions			
	millimeters		inches	
	min	max	min	max
A	2.650	2.950	0.104	0.116
A1	1.500	1.700	0.059	0.067
B	2.820	3.020	0.111	0.119
B1	0.950		0.037	
B2	0.300	0.500	0.012	0.020
C		1.250		0.049
C1	0	0.100	0.000	0.004
L	0.300	0.600	0.012	0.024
D	0.100	0.200	0.004	0.008
θ	0º	8º	0º	8º

TAPE AND REEL INFORMATION

REEL DIMENSIONS

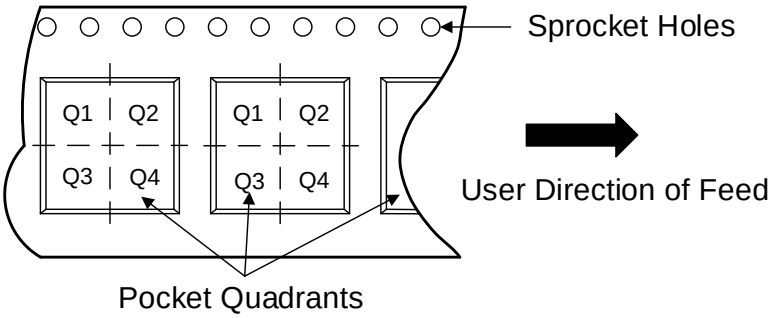


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component width thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadran
TS62373SOT235R	SOT-23-5L	5	3000	180.0	9.0	3.2	3.3	1.4	4.0	8.0	Q3

REVISION HISTORY

NOTE: Page numbers for previous revisions may be different from that of the current version.

2022/11/29 — REV KY0.0.0A to REV KY0.1.0A

Updated *Vs to GND Voltage* and *Input Voltage*……2

Add *APPLICATION NOTES & ADDITIONAL DETAILS*……6,7

2023/03/31 — REV KY0.1.0A to REV KY1.1.0A

Adjust Page Format……All pages

CONTACT INFORMATION

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